

GT93C46A



GT93C46A

Microwire

1K Bits

Serial EEPROM

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GT93C46A

Table of Contents

1. Features	3
2. General Description	3
3. Functional Block Diagram	4
4. Pin Configuration	5
4.1 8-Pin SOIC, TSSOP and PDIP	5
4.2 8-Lead UDFN	5
4.3 Pin Definition	5
5. Device Operation	6
5.1 Read	6
5.2 Write Enable	6
5.3 Write Disable	6
5.4 Write	6
5.5 Write All Memory	6
5.6 Erase	6
5.7 Erase All Memory	7
5.8 Power-On Reset	7
5.9 Instruction Set	7
5.10 Diagrams	8
6. Electrical Characteristics	11
6.1 Absolute Maximum Ratings	11
6.2 Operating Range	11
6.3 Capacitance	11
6.4 DC Electrical Characteristic	12
6.5 AC Electrical Characteristic	13
7. Ordering Information	14
8. Top Markings	15
8.1 SOIC Package	15
8.2 TSSOP Package	15
8.3 PDIP Package	15
8.4 UDFN Package	15
9. Package Information	16
9.1 SOIC	16
9.2 TSSOP	17
9.3 PDIP	18
9.4 UDFN	19
10. Revision History	20



GT93C46A

1. Features

- Industry-standard Microwire Interface
- Wide-voltage Operation
 - $V_{CC} = 1.8V$ to $5.5V$
- Speed
 - 1 MHz (1.8V), 2 MHz (2.5V), 3 MHz (5.5V)
- Standby current
 - 1uA (max.) 1.8V
- Operating current
 - 1mA (max.) 1.8V
- User Configured Memory Organization
 - 64x16-bit (ORG = V_{CC} or Floating)
 - or 128x8-bit (ORG = 0V)
- Self timed write cycle: 5 ms (max.)
- Hardware and software write protection
 - Defaults to write-disabled state at power-up
 - Software instructions for write-enable/disable
- CMOS technology
- Versatile, easy-to-use interface
 - Automatic erase-before-write
 - Programming status indicator
 - Byte, Word and chip single erasable
 - Chip select enables power savings
- Noise immunity on inputs, besides Schmitt trigger
- High-reliability
 - Endurance: 1 million cycles
 - Data retention: 100 years
- Packages: SOIC, TSSOP, PDIP and UDFN
- Lead-free, RoHS, Halogen free, Green

2. General Description

The GT93C46A is 1kb non-volatile serial EEPROM with memory array of 1,024 bits. The array can be organized as either 128 bytes of 8 bits or 64 words of 16 bits via the ORG control. Utilizing the CMOS design and process, these products provide low standby current and low power operations. The devices can operate in a wide supply voltage range from 1.8V to 5.5V, with frequency up to 3MHz.

When the ORG pin is connected to V_{CC} or floating, x16 is selected. Conversely, when it is connected to ground, x8 is chosen.

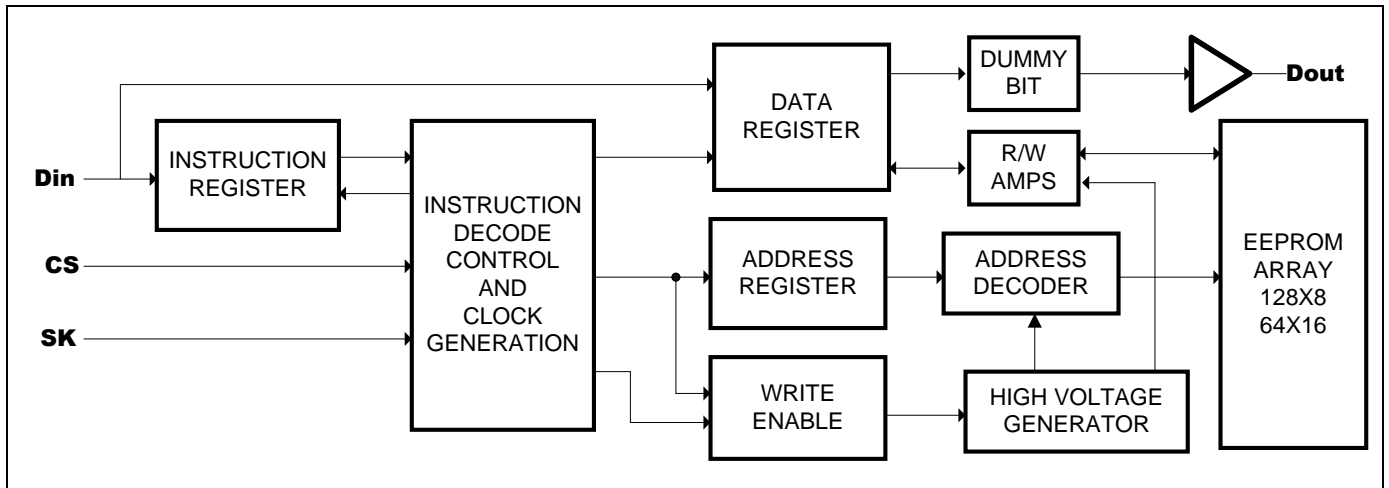
An instruction Op-code defines the various operations of

the devices, including read, write, and mode-enable functions. To protect against inadvertent data modification, all write and erase instructions are merely accepted while the device is in write enable mode. A selected x8 byte or x16 word can be modified with a single WRITE or ERASE instruction. Additionally, the WRITE ALL or ERASE ALL instruction can program or erase the entire array, respectively. Once a device begins its self-timed program procedure, the data out pin (D_{OUT}) can indicate the READY/BUSY status by raising chip select (CS). The devices can output any number of consecutive bytes/words using a single READ instruction.



GT93C46A

3. Functional Block Diagram

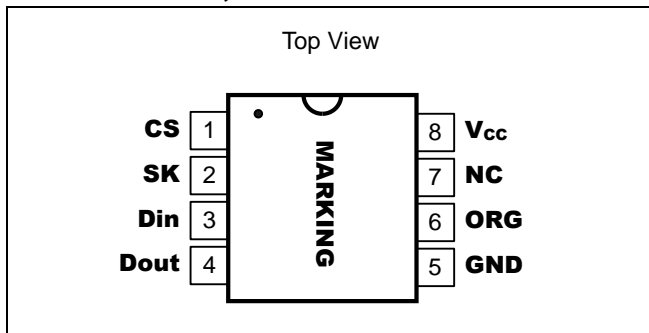




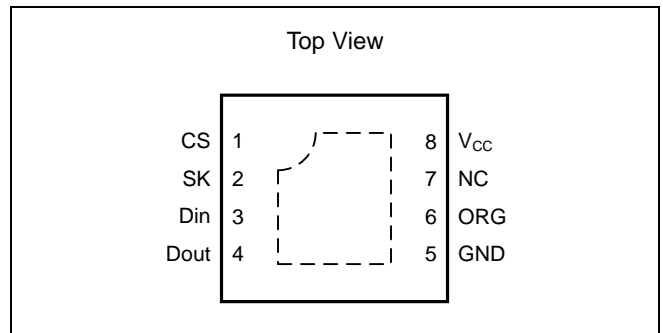
GT93C46A

4. Pin Configuration

4.1 8-Pin SOIC, TSSOP and PDIP



4.2 8-Lead UDFN



4.3 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	CS	I	Chip Select
2	SK	I	Serial Data Clock
3	DIN	I	Serial Data Input
4	DOUT	O	Serial Data Output
5	GND	-	Ground
6	ORG	I	Organization Select
7	NC	-	Not Connect
8	V _{CC}	-	Supply Voltage



GT93C46A

5. Device Operation

The GT93C46A is controlled by a set of instructions which are clocked-in serially on the D_{IN} pin. Before each low-to-high transition of the clock (SK), the CS pin must have already been raised to HIGH, and the D_{IN} value must be stable at either LOW or HIGH. Each instruction begins with a start bit of the logical “1” or HIGH. Following this are the Op-code, address field, and data, if appropriate. The clock signal may be held stable at any moment to suspend the device at its last state, allowing clock speed flexibility. Upon completion of bus communication, CS would be pulled LOW. The device then would enter Standby mode if no internal programming is underway.

5.1 Read

The READ instruction is the only instruction that outputs serial data on the D_{OUT} pin. After the read instruction and address have been decoded, data is transferred from the selected memory array into a serial shift register. (Please note that one logical “0” bit precedes the actual 8 or 16-bit output data string.) The output on D_{OUT} changes during the low-to-high transitions of SK (see Figure 5.10-2).

The GT93C46A is designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 8 or 16 bits of the addressed register have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the chip select (CS) control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

5.2 Write Enable

The write enable (WEN) instruction must be executed before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter, the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (See Figure 5.10-3) (Note: Chip select must remain LOW until

V_{CC} reaches its operational value.)

5.3 Write Disable

The write disable (WDS) instruction disables all programming capabilities. This protects the entire device against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation.

5.4 Write

The WRITE instruction writes 8 or 16 bits of data into the specified memory location. After the last data bit has been applied to D_{IN} , and before the next rising edge of SK, CS must be brought LOW. If the device is write-enabled, then the falling edge of CS initiates the self-timed programming cycle (see WEN). If CS is brought HIGH, after a minimum wait of 200 ns after the falling edge of CS (T_{CS}) D_{OUT} will indicate the READY/BUSY status of the chip. Logical “0” means programming is still in progress; logical “1” means the selected memory array has been written, and the part is ready for another instruction (see Figure 5.10-4). The READY/BUSY status will not be available if the CS input goes HIGH after the end of the self-timed programming cycle (T_{wp}).

5.5 Write All Memory

The write all (WRALL) instruction programs entire memory with the data pattern specified in the instruction. As with the WRITE instruction, the falling edge of CS must occur to initiate the self-timed programming cycle. If CS is then brought HIGH after a minimum wait of 200 ns (T_{CS}), the D_{OUT} pin indicates the READY/BUSY status of the chip (see Figure 5.10-5).

5.6 Erase

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of T_{CS} , will cause D_{OUT} to indicate the READ/BUSY status of the chip: a logical “0” indicates programming is still in progress; a logical “1” indicates the erase cycle is complete



GT93C46A

and the part is ready for another instruction (see Figure 5.10-7).

5.7 Erase All Memory

Full chip erase (ERAL) is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical “1” (see Figure 5.10-8).

5.8 Power-On Reset

The device incorporates a Power-On Reset (POR) circuitry which protects the internal logic against powering up into a wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This POR feature protects the device being ‘brown-out’ due to a sudden power loss or power cycling.

In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset (POR) circuit is embedded. During power-up, the device does not respond to any instruction until V_{CC} has reached a minimum stable level above the reset threshold voltage. Once V_{CC} passes the POR threshold, the device is reset and enters in Standby mode. This can also avoid any inadvertent Write operations during power-up stage. During power-down process, the device must enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will enter standby mode after current operation completes, provided that no internal write operation is in progress.

5.9 Instruction Set

Instruction ^[2]	Start Bit	OP Code	8-bit Organization (ORG = GND)			16-bit Organization (ORG = V_{CC} or Floating)		
			Address ^[1]	Data ^[1]	Required Clock Cycles	Address ^[1]	Data ^[1]	Required Clock Cycles
WDS (Write Disable)	1	00	00x xxxx	—	10	00 xxxx	—	9
WEN (Write Enable)	1	00	11x xxxx	—	10	11 xxxx	—	9
ERAL (Erase All Memory)	1	00	10x xxxx	—	10	10 xxxx	—	9
WRAL (Write All Memory)	1	00	01x xxxx	(D ₇ -D ₀)	18	01 xxxx	(D ₁₅ -D ₀)	25
WRITE	1	01	A ₆ -A ₀	(D ₇ -D ₀)	18	A ₅ -A ₀	(D ₁₅ -D ₀)	25
READ	1	10	A ₆ -A ₀	—		A ₅ -A ₀	—	
ERASE	1	11	A ₆ -A ₀	—	10	A ₅ -A ₀	—	9

Notes: ^[1] x = Don't care bit.

^[2] Exact number of clock cycles is required for each Op-code instruction.



5.10 Diagrams

Figure 5.10-1. Synchronous Data Timing

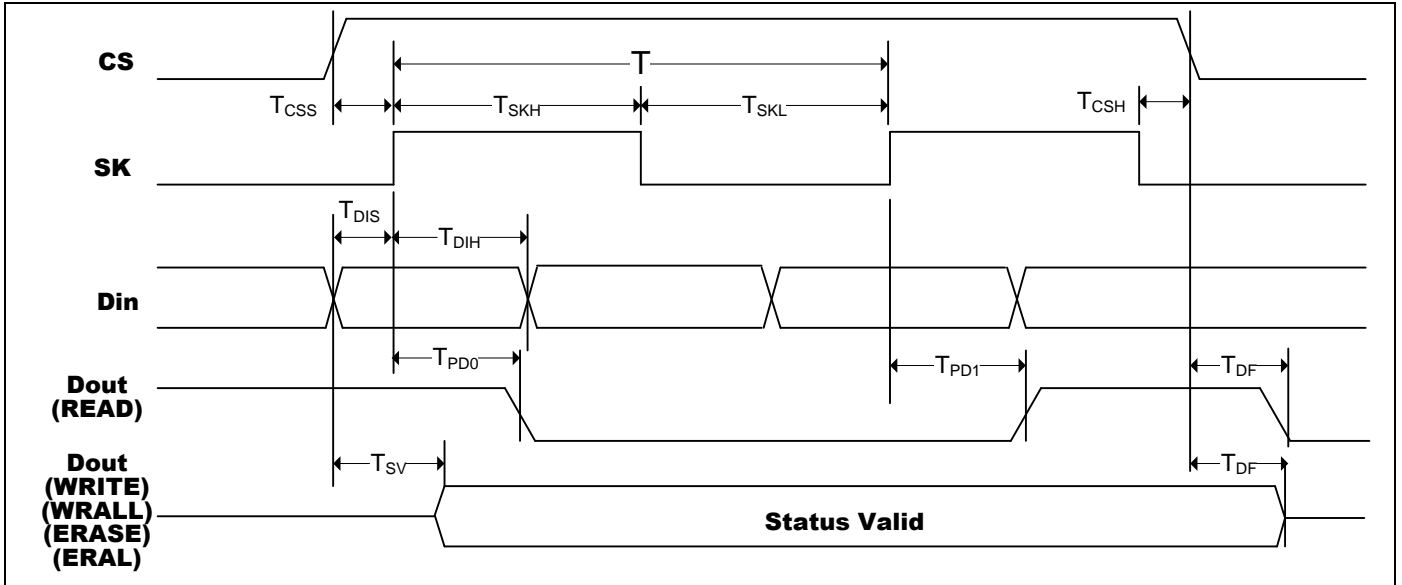
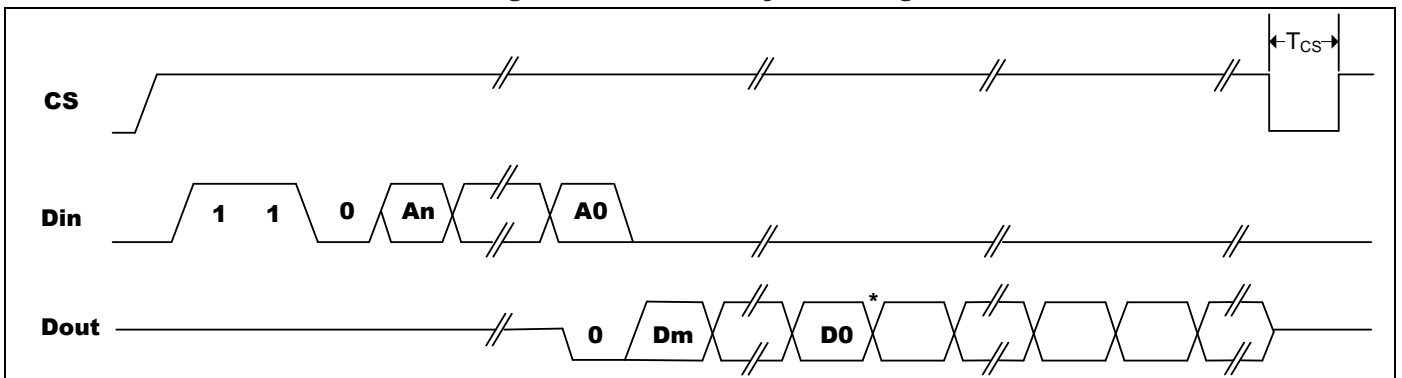


Figure 5.10-2. Read Cycle Timing



Notes: * Address Pointer Cycles to the Next Register

Figure 5.10-3. Write Enable (WEN) Cycle Timing

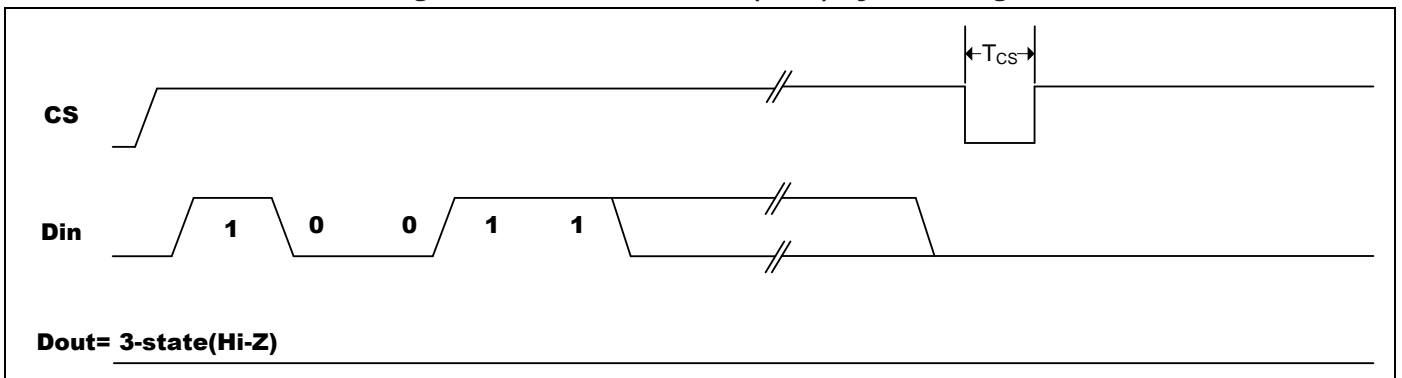
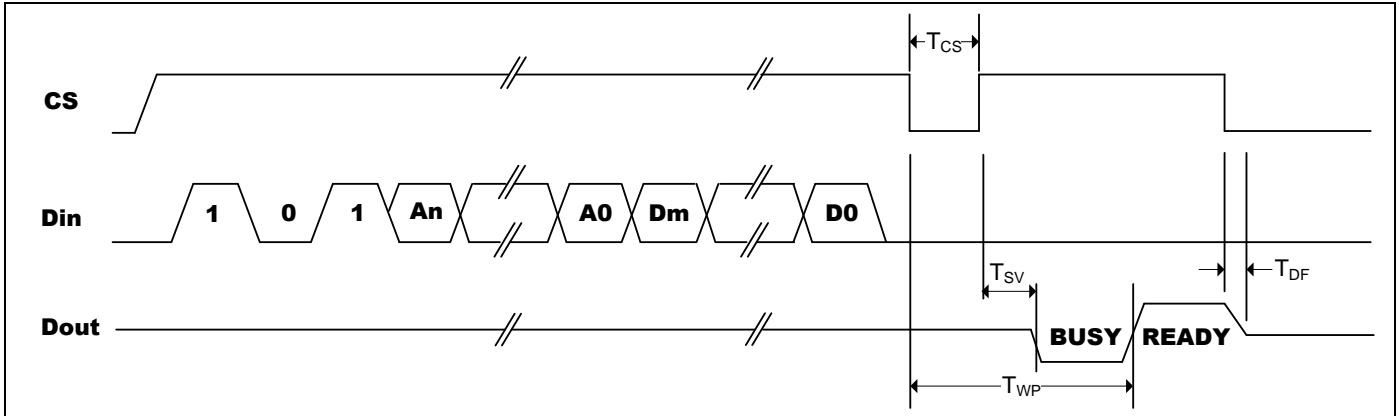




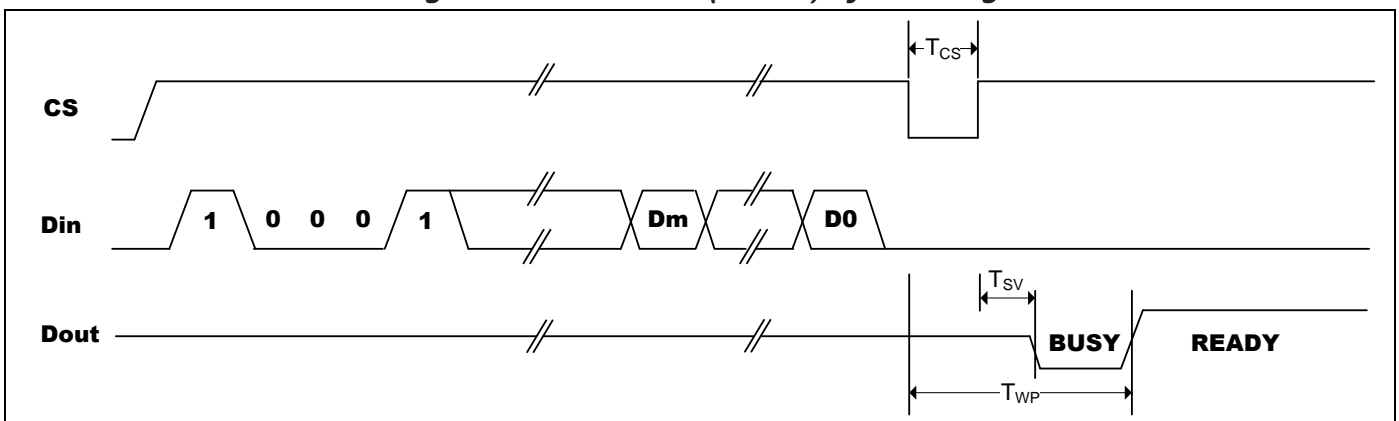
Figure 5.10-4. Write (Write) Cycle Timing



Notes: ^[1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.

^[2] To determine data bits $A_n - A_0$ and data bits $D_m - D_0$, see Instruction Set for the appropriate device.

Figure 5.10-5. Write All (WRALL) Cycle Timing



Notes: ^[1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.

^[2] To determine data bits $D_m - D_0$, see Instruction Set for the appropriate device.

Figure 5.10-6. Write Disable (WDS) Timing

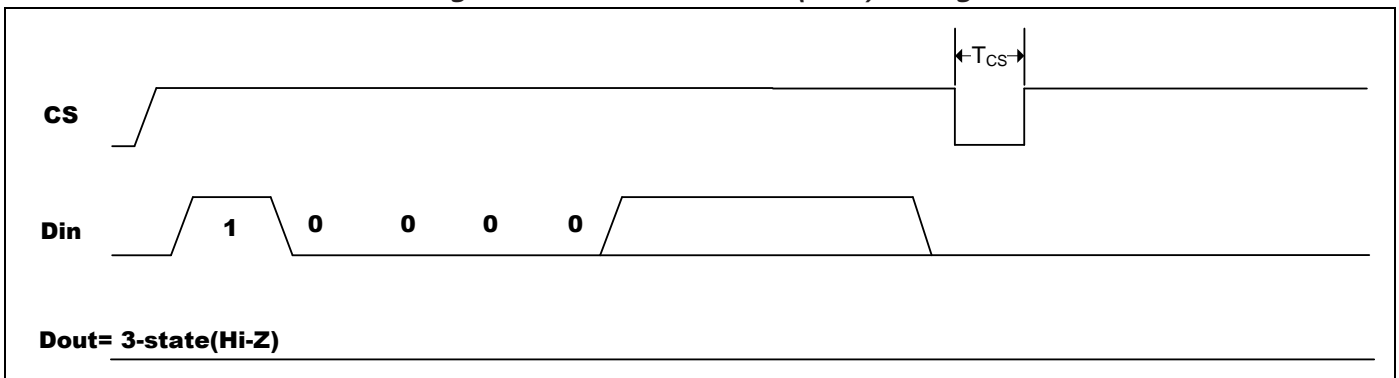
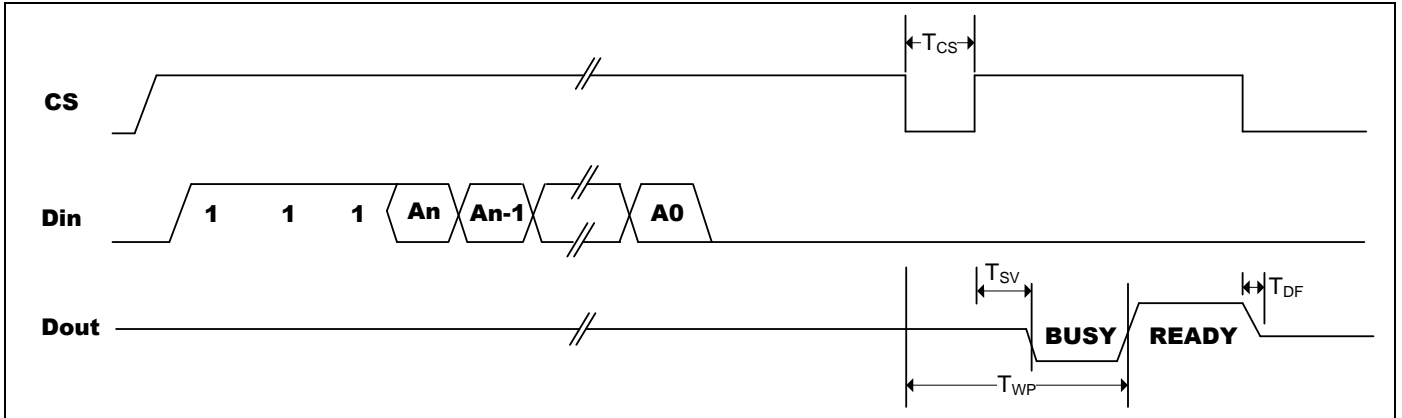




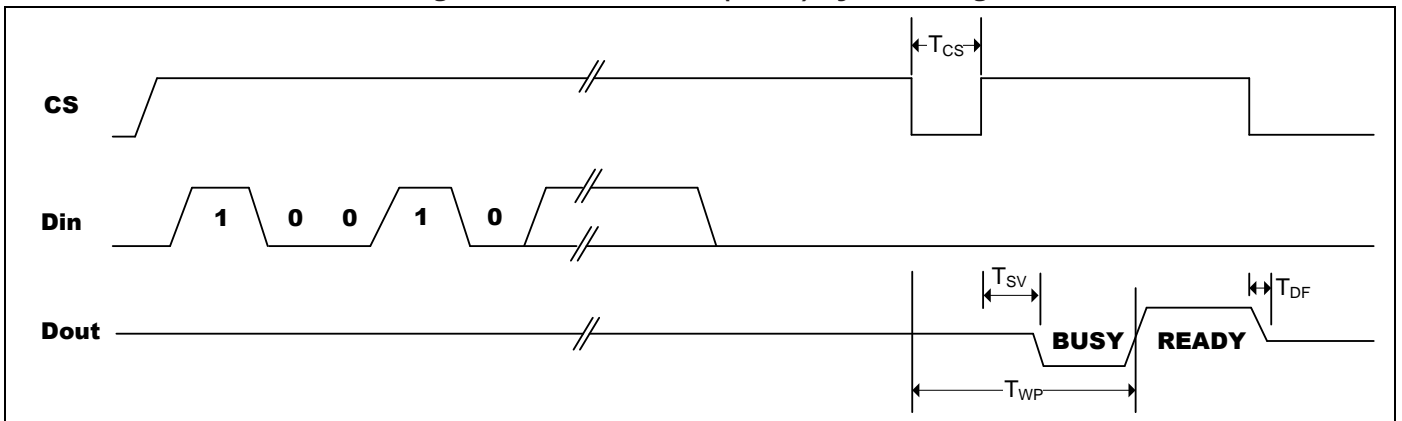
Figure 5.10-7. Erase (Erase) Cycle Timing



Notes: ^[1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.

^[2] To determine data bits $A_n - A_0$, see Instruction Set for the appropriate device.

Figure 5.10-8. Erase All (ERAL) Cycle Timing



Notes: ^[1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.

^[2] To determine data bits $A_n - A_0$, see Instruction Set for the appropriate device.



GT93C46A

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _S	Supply Voltage	-0.5 to + 6.5	V
V _P	Voltage on Any Pin	-0.5 to + 6.5	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Operating Range

Range	Ambient Temperature (T _A)	V _{CC}
Industrial	-40°C to +85°C	1.8V to 5.5V

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

6.3 Capacitance

Symbol	Parameter ^[1, 2]	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{I/O}	Input / Output Capacitance	V _{I/O} = 0V	8	pF

Notes: ^[1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

^[2] Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.



GT93C46A

6.4 DC Electrical Characteristic

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 1.8\text{V} \sim 5.5\text{V}$

Symbol	Parameter [1]	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		1.8	5.5	V
V_{OL1}	Output LOW Voltage	$V_{CC} = 1.8\text{V} \sim 5.5\text{V}$, $I_{OL} = 100 \mu\text{A}$	—	0.2	V
V_{OL2}	Output LOW Voltage	$V_{CC} = 2.5\text{V} \sim 5.5\text{V}$, $I_{OL} = 2.1 \text{mA}$	—	0.4	V
V_{OH1}	Output HIGH Voltage	$V_{CC} = 1.8\text{V} \sim 5.5\text{V}$, $I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
V_{OH2}	Output HIGH Voltage	$V_{CC} = 2.5\text{V} \sim 5.5\text{V}$, $I_{OH} = -0.4\text{mA}$	2.4	—	V
V_{IH1}	Input HIGH Voltage	1.8V to 5.5V	$0.7 \cdot V_{CC}$	$V_{CC} + 1$	V
V_{IH2}	Input HIGH Voltage	2.5V to 5.5V	2	$V_{CC} + 1$	V
V_{IL1}	Input LOW Voltage	1.8V to 5.5V	-0.3	$0.3 \cdot V_{CC}$	V
V_{IL2}	Input LOW Voltage	2.5V to 5.5V	-0.3	0.8	V
I_{LI}	Input Leakage Current	$V_{IN} = 0\text{V}$ to V_{CC} (CS, SK, D_{IN} , ORG)	0	2.5	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0\text{V}$ to V_{CC} , CS = 0V	0	2.5	μA

Power Supply Characteristics

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 1.8\text{V} \sim 5.5\text{V}$

Symbol	Parameter [1]	V_{CC}	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage			1.8		5.5	V
I_{SB1}	Standby current	1.8	CS = GND, SK = GND, ORG = V_{CC} or Floating (x16), $D_{IN} = V_{CC}$ or GND	—	0.1	1	μA
		2.5		—	0.3	1	μA
		5.5		—	0.5	1	μA
I_{SB2}	Standby current	1.8	CS = GND, SK = GND, ORG = GND (x8), $D_{IN} = V_{CC}$ or GND	—	0.4	1	μA
		2.5		—	6	10	μA
		5.5		—	10	15	μA
$I_{CC-Read}$	Read current	1.8	CS = V_{IH} , SK = 1 MHz	—		0.5	mA
		2.5	CS = V_{IH} , SK = 2 MHz	—		0.5	mA
		5.5	CS = V_{IH} , SK = 3 MHz	—		1	mA
$I_{CC-Write}$	Write current	1.8	CS = V_{IH} , SK = 1 MHz	—		1	mA
		2.5	CS = V_{IH} , SK = 2 MHz	—		1	mA
		5.5	CS = V_{IH} , SK = 3 MHz	—		2	mA



GT93C46A

6.5 AC Electrical Characteristic

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, Supply voltage = 1.8V to 5.5V

Symbol	Parameter ^{[1] [2]}	1.8V ≤ V _{CC} < 2.5V		2.5V ≤ V _{CC} < 4.5V		4.5V ≤ V _{CC} ≤ 5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F _{SCK}	SCK Clock Frequency	0	1	0	2	0	3	MHz
T _R	Input Rise Time	—	10	—	10	—	10	ns
T _F	Input Fall Time	—	10	—	10	—	10	ns
T _{SKH}	SK High Time	250	—	200	—	200	—	ns
T _{SKL}	SK Low Time	250	—	200	—	100	—	ns
T _{CS}	Minimum CS LOW Time	250	—	200	—	200	—	ns
T _{CSS}	CS Setup Time	200	—	100	—	50	—	ns
T _{CSH}	CS Hold Time	0	—	0	—	0	—	ns
T _{DIS}	D _{IN} Setup Time	100	—	50	—	50	—	ns
T _{DIH}	D _{IN} Hold Time	50	—	50	—	50	—	ns
T _{PD1}	Output Delay to "1"	—	400	—	200	—	100	ns
T _{PD0}	Output Delay to "0"	—	400	—	200	—	100	ns
T _{SV}	CS to Status Valid	—	400	—	200	—	200	ns
T _{DF}	CS to D _{OUT} in 3-state	—	200	—	100	—	100	ns
T _{WP}	Write Cycle Time	—	10	—	5	—	5	ms

Notes: ^[1] The parameters are characterized but not 100% tested.

^[2] AC measurement conditions:

C_L = 100 pF

Input pulse voltages: Per V_{IL} and V_{IH} spec

Input rise and fall times: ≤ 10 ns

Timing reference voltages: half V_{CC} level



GT93C46A

7. Ordering Information

Industrial Grade: -40°C to +85°C, Lead-free

Voltage Range	Part Number*	Package (8-pin)*
1.8V to 5.5V	GT93C46A-2GLI-TR	150-mil SOIC
	GT93C46A-2ZLI-TR	3 x 4.4 mm TSSOP
	GT93C46A-2PLI	300-mil PDIP
	GT93C46A-2UDLI-TR	2 x 3 x 0.55 mm UDFN

*

1. Contact Giantec Sales Representatives for availability and other package information.
2. The listed part numbers are packed in tape and reel "-TR" (4K per reel). UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).



GT93C46A

8. Top Markings

8.1 SOIC Package



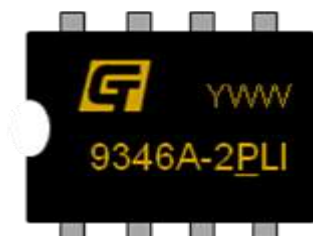
GT: Giantec Logo
346A-2GLI: Part Number GT93C46A-2GLI-TR
YWW: Date Code, Y=year, WW=week

8.2 TSSOP Package



GT: Giantec Logo
346A-2ZLI: Part Number, GT93C46A-2ZLI-TR
YWW: Date Code, Y=year, WW=week

8.3 PDIP Package



GT: Giantec Logo
9346A-2PLI: Part Number GT93C46A-2PLI
YWW: Date Code, Y=year, WW=week

8.4 UDFN Package



GT: Giantec Logo
30A: Part Number GT93C46A-2UDLI-TR
YWW: Date Code, Y=year, WW=week

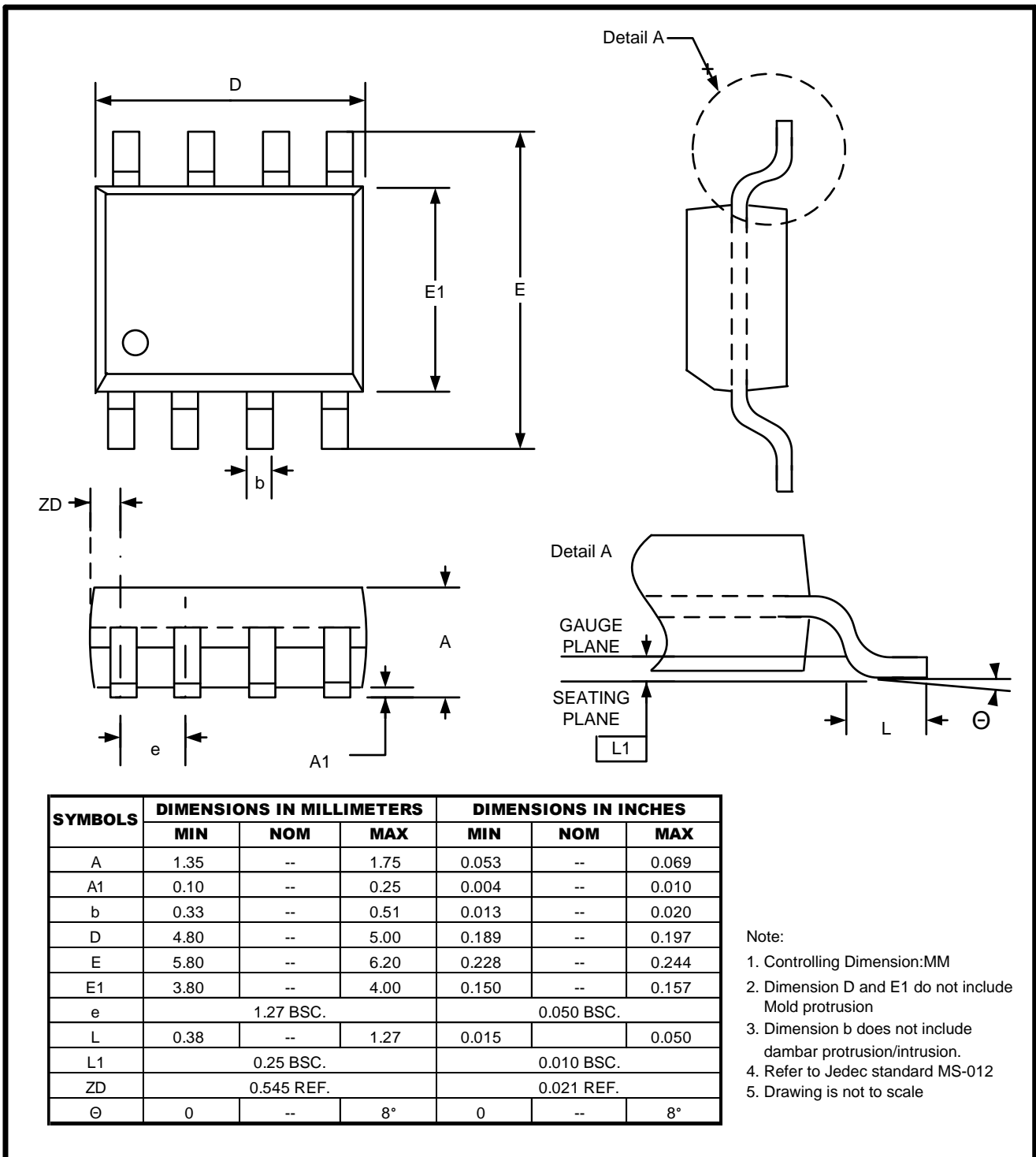


GT93C46A

9. Package Information

9.1 SOIC

8L 150mil SOIC Package Outline

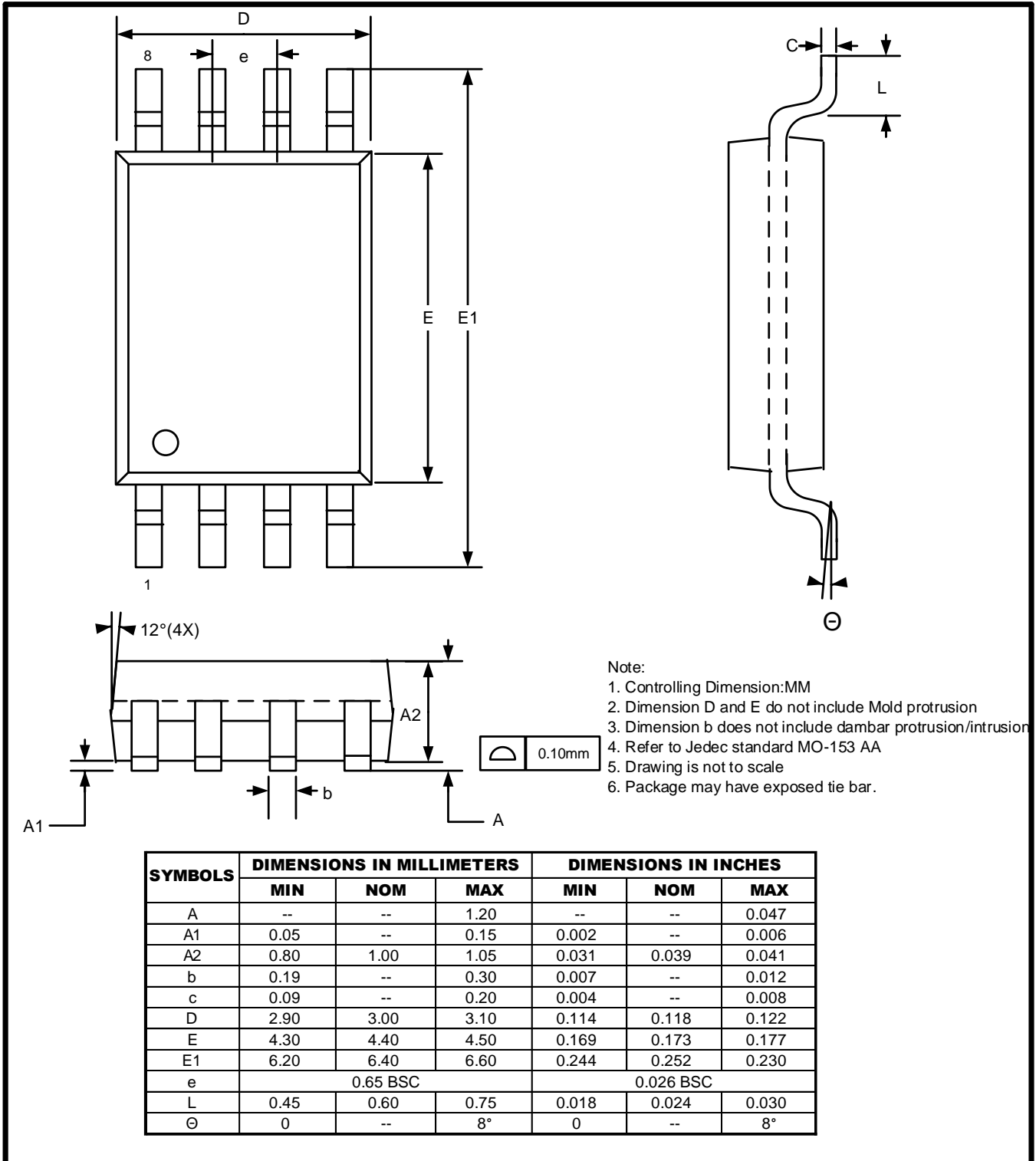




GT93C46A

9.2 TSSOP

8L 3x4.4mm TSSOP Package Outline

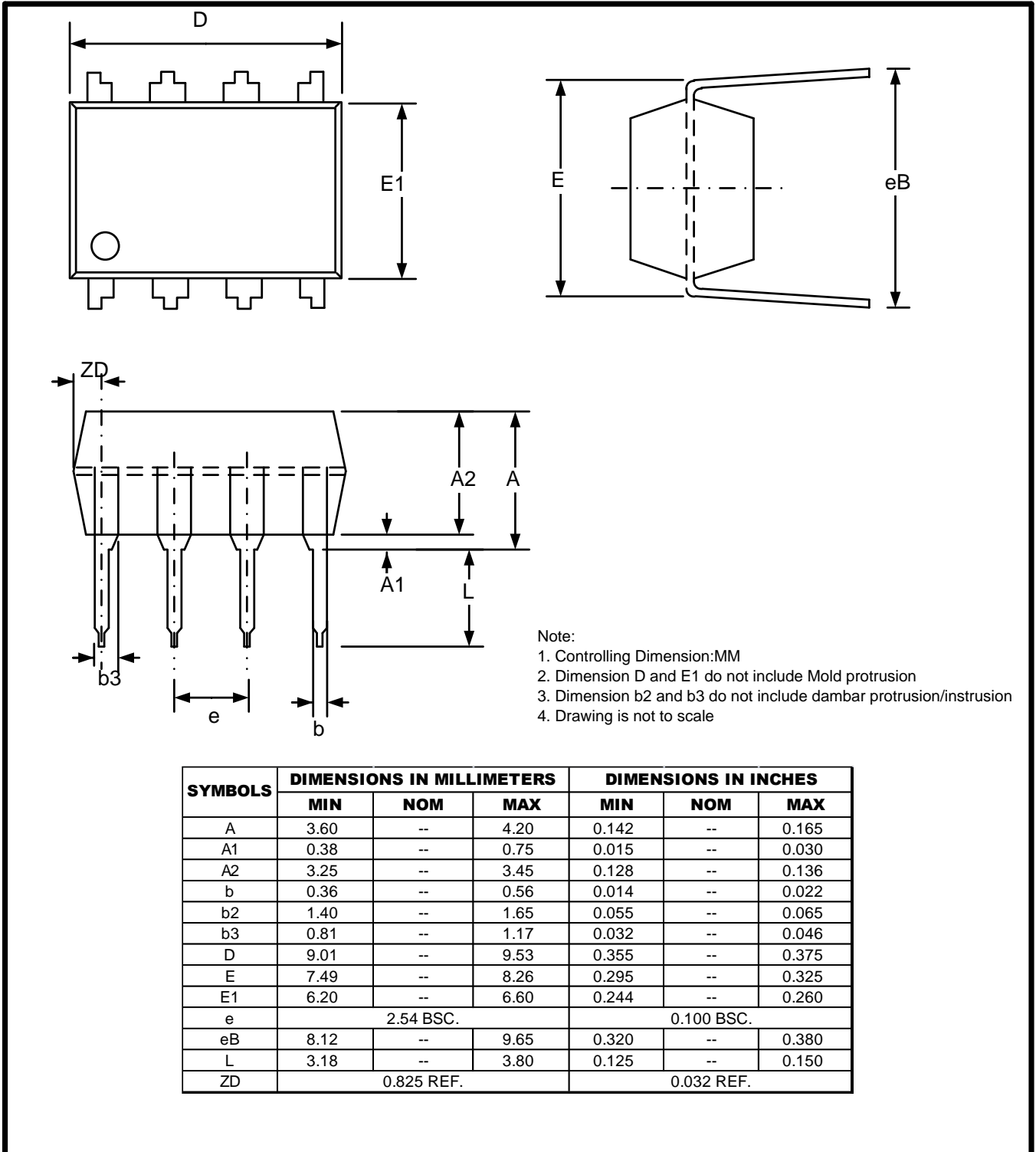




GT93C46A

9.3 PDIP

8L 300mil PDIP Package Outline

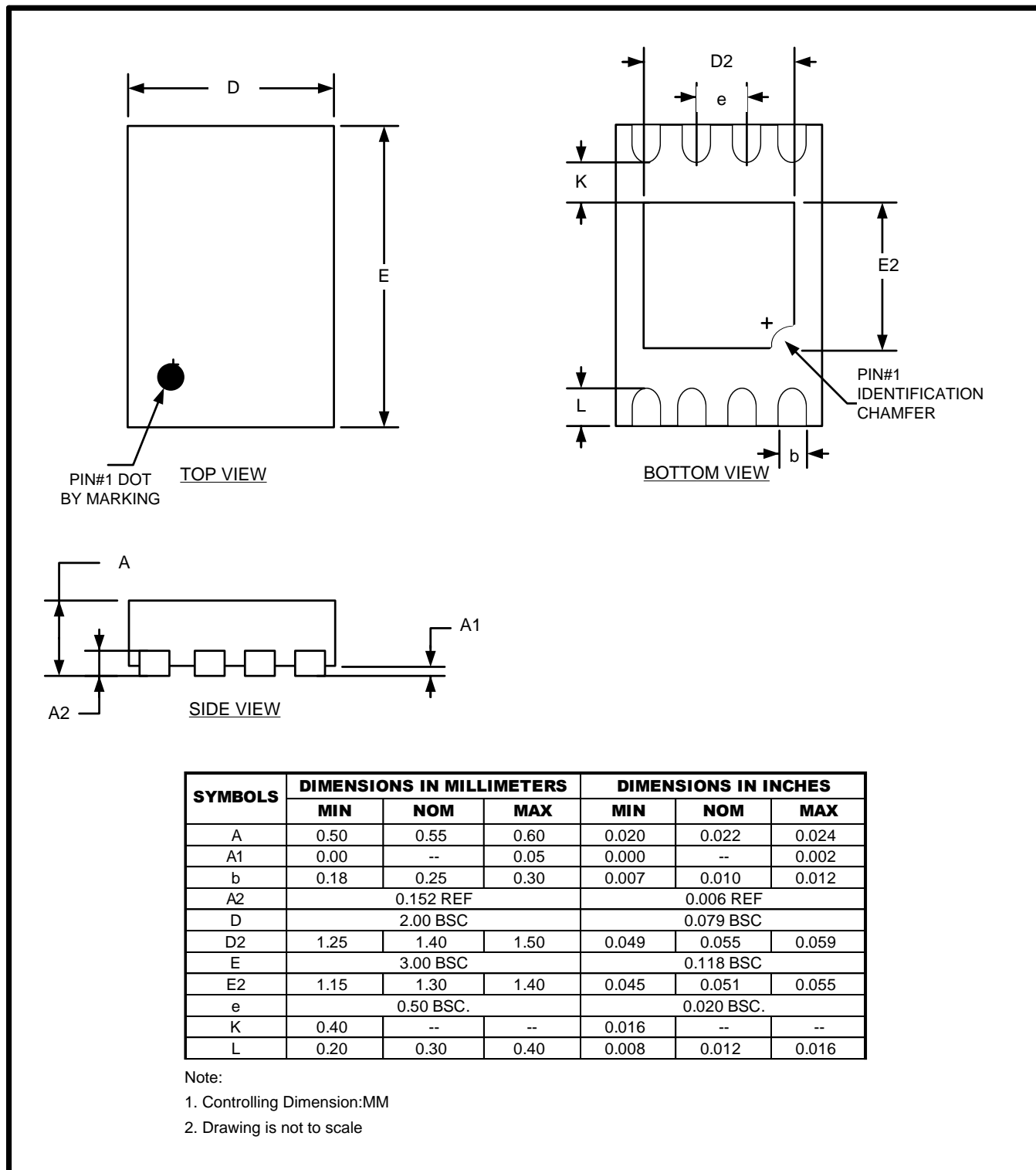




GT93C46A

9.4 UDFN

8L 2x3mm UDFN Package Outline





GT93C46A

10. Revision History

Revision	Date	Descriptions
A0	Nov. 2010	Initial version
A1	Jun. 2011	New datasheet format
A2	Oct. 2013	Update Cu wire top marking
C3	Oct. 2013	Revise SOIC/SOP to SOIC
C4	Jul. 2019	Update TSSOP POD and VP