GT7161

1.5M, Zero-Drift, CMOS, Rail-to-Rail Operational Amplifier　　Advanced

1. Features

- Single-Supply Operation from +2.2V ~ +5.5V
- Rail-to-Rail Input / Output
- Gain-Bandwidth Product: 1.5 MHz (Typ.)
- Low Input Bias Current: 80pA (Typ.)
- Low Offset Voltage: 15µV (Max.)
- Zero Drift: 0.05µV/^{o}C (Max.)
- Quiescent Current: 320µA (Typ.)
- Operating Temperature: -40°C ~ +125°C
- Available in SOT23-5 and SOP8 Packages

2. General Description

The GT7161 amplifier is single supply, micro-power, zero-drift CMOS operational amplifier, the amplifier offer bandwidth of 1.5MHz, rail-to-rail inputs and outputs, and single-supply operation from 2.2V to 5.5V. GT7161 uses chopper stabilized technique to provide very low offset voltage (less than 15µV maximum) and near zero drift over temperature. Low quiescent supply current of 320µA and very low input bias current of 80pA make the devices an ideal choice for low offset, low power consumption and high impedance applications. The single GT7161 is available in space-saving, SOT23-5 and SOP-8 package. The extended temperature range of -40^{o}C to +125^{o}C over all supply voltages offers additional design flexibility.

3. Applications

- Portable Equipment
- Mobile Communications
- Smoke Detector
- Sensor Interface
- Medical Instrumentation
- Battery-Powered Instruments
- Handheld Test Equipment

4. Pin Configuration

4.1 GT7161 SOT23-5 and SOP8 (Top View)

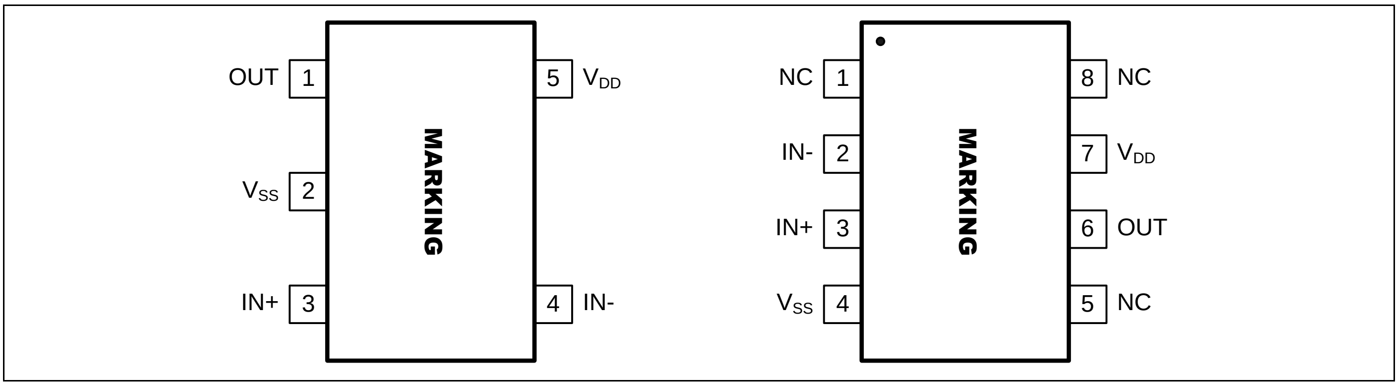


Figure 1. Pin Assignment Diagram (SOP23-5 and SOP8 Package)

Note: Please see section "**Part Markings**" for detailed Marking Information.

5. Application Information

5.1 Size

GT7161 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. The small footprints of the GT7161 series packages save space on printed circuit boards and enable the design of smaller electronic products.

5.2 Power Supply Bypassing and Board Layout

GT7161 series operates from a single 2.2V to 5.5V supply or dual ±1.1V to ±2.75V supplies. For best performance, a 0.1μF ceramic capacitor should be placed close to the V_{DD} pin in single supply operation. For dual supply operation, both V_{DD} and V_{SS} supplies should be bypassed to ground with separate 0.1μF ceramic capacitors.

5.3 Low Supply Current

The low supply current (typical 320μA) of GT7161 series will help to maximize battery life. They are ideal for battery powered systems

5.4 Operating Voltage

GT7161 series operate under wide input supply voltage (2.2V to 5.5V). In addition, all temperature specifications apply from -40 °C to +125 °C. Most behavior remains unchanged throughout the full operating voltage range. These guarantees ensure operation throughout the single Li-Ion battery lifetime

5.5 Rail-to-Rail Input

The input common-mode range of GT7161 series extends 100mV beyond the supply rails (V_{SS}-0.1V to V_{DD}+0.1V). This is achieved by using complementary input stage. For normal operation, inputs should be limited to this range.

Normally, input bias current is about 80pA; however, if the input voltages exceed the power supplies, excessive current can flow into or out of the pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This limitation can be accomplished with an 5kΩ series input resistor.

5.6 Rail-to-Rail Output

Rail-to-Rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating in low supply voltages. The output voltage of GT7161 series can typically swing to less than 10mV from supply rail in light resistive loads (>100kΩ), and 60mV of supply rail in moderate resistive loads (10kΩ).

5.7 Capacitive Load Tolerance

The GT7161 series can directly drive 250pF capacitive load in unity-gain without oscillation. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. In unity-gain configurations, the capacitive load drive can be improved by inserting an isolation resistor R_{ISO} in series with the capacitive load, as shown in ***Figure 2***.

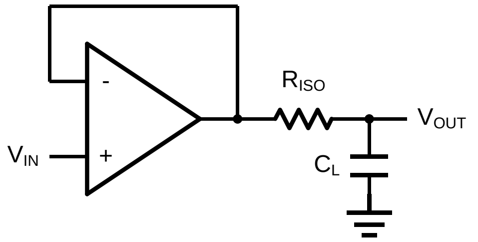


Figure 2. Indirectly Driving a Capacitive Load Using Isolation Resistor

The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. However, if there is a resistive load R_L in parallel with the capacitive load, a voltage divider (proportional to R_{ISO}/R_L) is formed, this will result in a gain error.

The circuit in ***Figure 3*** is an improvement to the one in ***Figure 2***. R_F provides the DC accuracy by feed-forward the V_{IN} to R_L. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving the phase margin in the overall feedback loop. Capacitive drive can be increased by increasing the value of C_F. This in turn will slow down the pulse response.

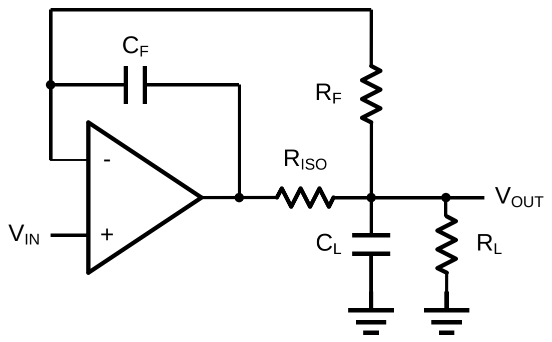


Figure 3. Indirectly Driving a Capacitive Load with DC Accuracy

5.8 Differential amplifier

The differential amplifier allows the subtraction of two input voltages or cancellation of a signal common the two inputs. It is useful as a computational amplifier in making a differential to single-end conversion or in rejecting a common mode signal. ***Figure 4.*** shown the differential amplifier using GT7161.

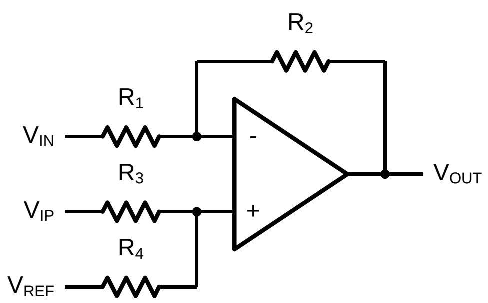


Figure 4. Differential Amplifier

$$V_{OUT} = \left(\frac{R_1+R_2}{R_3+R_4}\right)\frac{R_4}{R_1}V_{IN} - \frac{R2}{R1}V_{IP} + \left(\frac{R_1+R_2}{R_3+R_4}\right)\frac{R_3}{R_1}V_{REF}$$

If the resistor ratios are equal (i.e. $R_1=R_3$ and $R_2=R_4$), then

$$V_{OUT} = \frac{R_2}{R_1}(V_{IP} - V_{IN}) + V_{REF}$$

5.9 Instrumentation Amplifier

The input impedance of the previous differential amplifier is set by the resistors R1, R2, R3, and R4. To maintain the high input impedance, one can use a voltage follower in front of each input as shown in the following two instrumentation amplifiers.

5.10 Three-Op-Amp Instrumentation Amplifier

The triple GT7161 can be used to build a three-op-amp instrumentation amplifier as shown in ***Figure 5***.

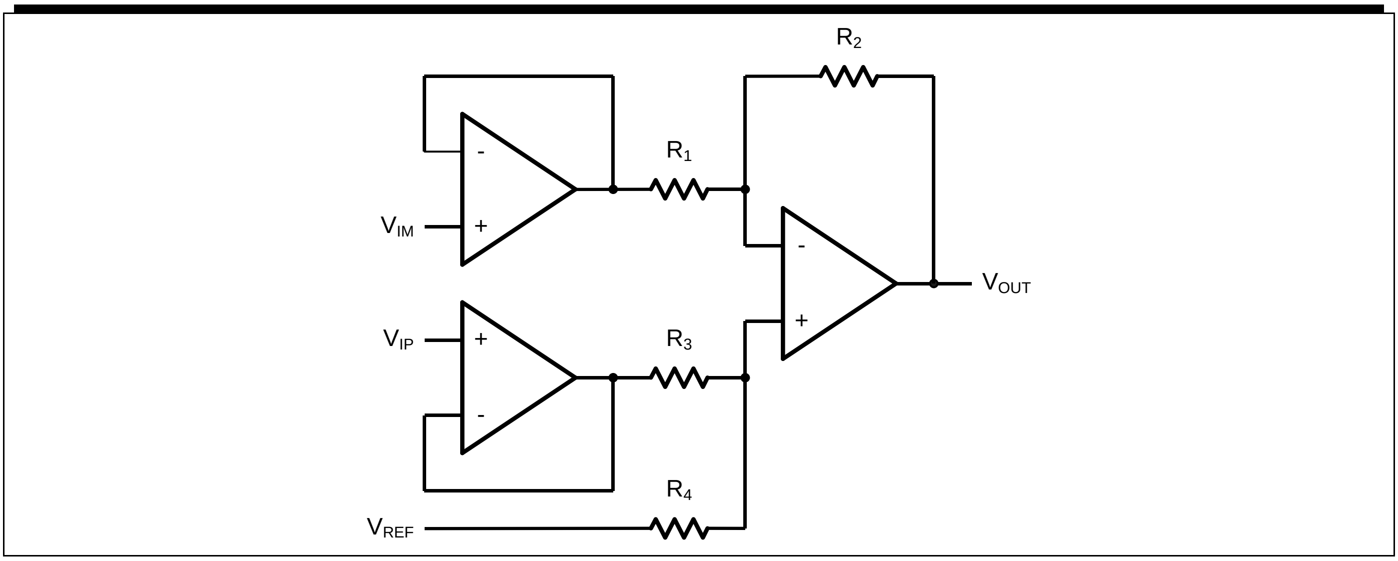


Figure 5. Three-Op-Amp Instrumentation Amplifier

The amplifier in ***Figure 5*** is a high input impedance differential amplifier with gain of R_2/R_1. The two differential voltage followers assure the high input impedance of the amplifier.

$$Vo = \left(1+\frac{R_4}{R_3}\right)(V_{IP} - V_{IN})$$

5.11 Two-Op-Amp Instrumentation Amplifier

GT7161 can also be used to make a high input impedance two-op-amp instrumentation amplifier as shown in ***Figure 6***.

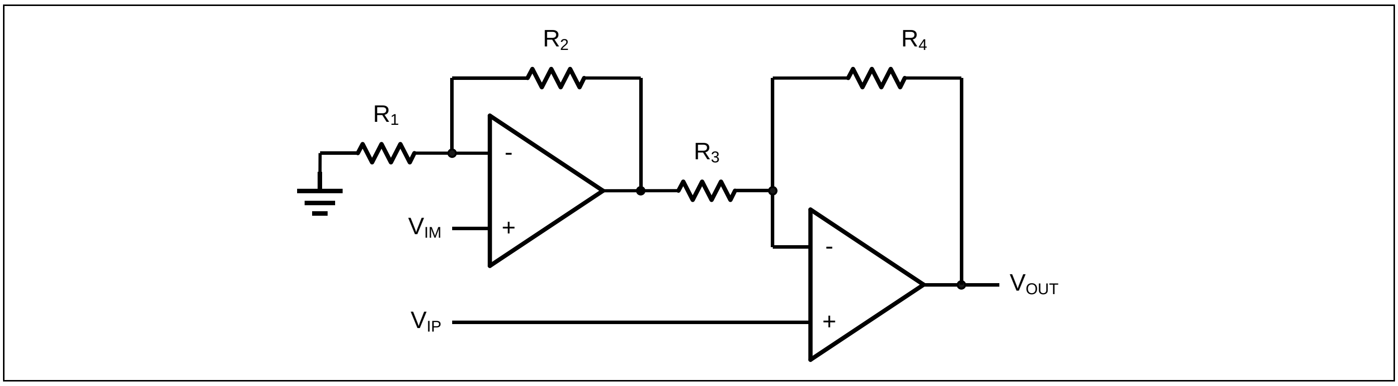


Figure 6. Two-Op-Amp Instrumentation Amplifier

Where R_1=R_3 and R_2=R_4. If all resistors are equal, then $V_o=2(V_{IP}-V_{IN})$

5.12 Single-Supply Inverting Amplifier

The inverting amplifier is shown in Figure 6. The capacitor C_1 is used to block the DC signal going into the AC signal source V_{IN}. The value of R_1 and C_1 set the cut-off frequency to $f_C=1/(2\pi R_1C_1)$. The DC gain is defined by $V_{OUT}=-(R_2/R_1)V_{IN}$

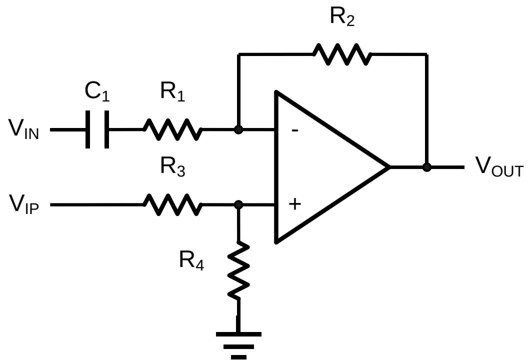


Figure 7. Single Supply Inverting Amplifier

5.13 Low Pass Active Filter

The low pass active filter is shown in ***Figure 8***. The DC gain is defined by $-R_2/R_1$. The filter has a -20dB/decade roll-off after its corner frequency $f_C=1/(2\pi R_3C_1)$.

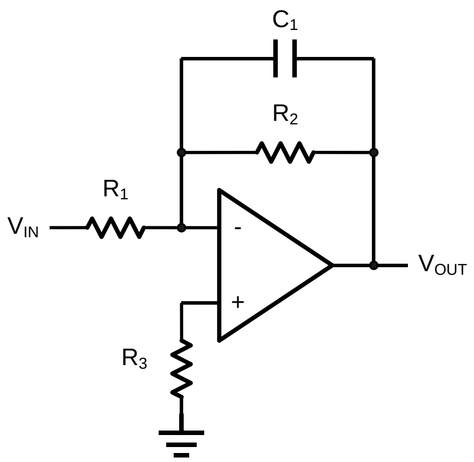


Figure 8. Low Pass Active Filter

5.14 Sallen-Key 2nd Order Active Low-Pass Filter

GT7161 can be used to form a 2nd order Sallen-Key active low-pass filter as shown in ***Figure 9***. The transfer function from V_{IN} to V_{OUT} is given by

$$\frac{V_{OUT}}{V_{IN}}(S)=\frac{\frac{1}{C_1C_2R_1R_2}A_{LP}}{S^2+S\left(\frac{1}{C_1R_1}+\frac{1}{C_1R_2}+\frac{1}{C_2R_2}-\frac{A_{LP}}{C_2R_2}\right)+\frac{1}{C_1C_2R_1R_2}}$$

Where the DC gain is defined by $A_{LP}=1+R_3/R_4$, and the corner frequency is given by

$$\omega_C=\sqrt{\frac{1}{C_1C_2R_1R_2}}$$

The pole quality factor is given by

$$\frac{\omega C}{Q}=\frac{1}{C_1R_1}+\frac{1}{C_1R_2}+\frac{1}{C_2R_2}-\frac{A_{LP}}{C_2R_2}$$

Let R1=R2=R and C1=C2=C, the corner frequency and the pole quality factor can be simplified as below

$$\omega_C=\frac{1}{CR}$$

And $Q=2-R_3/R_4$

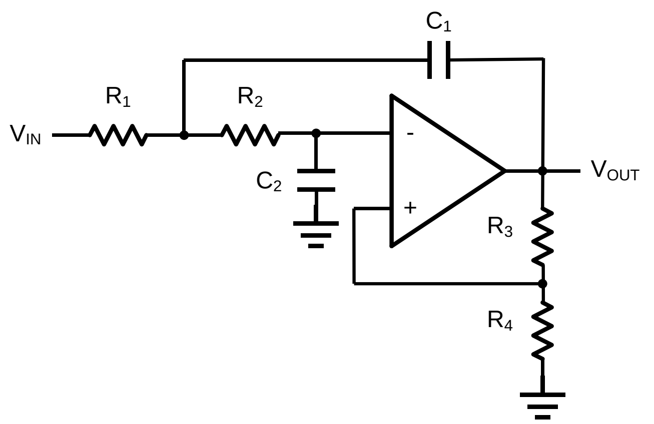


Figure 9. Sanllen-Key 2nd Order Active Low-Pass Filter

5.15 Sallen-Key 2nd Order high-Pass Active Filter

The 2nd order Sallen-key high-pass filter can be built by simply interchanging those frequency selective components R_1, R_2, C_1, and C_2 as shown in ***Figure 10***.

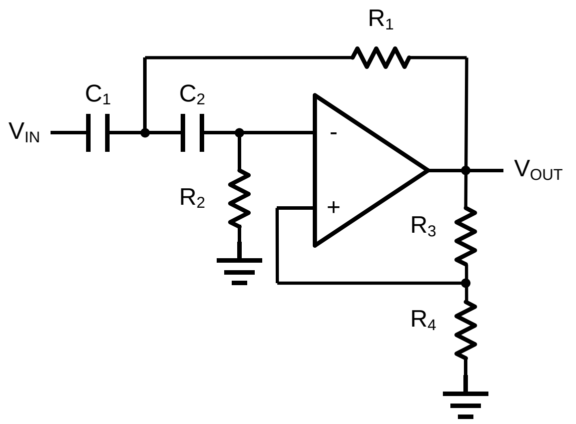


Figure 10. Sanllen-Key 2nd Order Active High-Pass Filter

$$\frac{V_{OUT}}{V_{IN}}(S)=\frac{S^2A_{HP}}{S^2+S\left(\frac{1}{C_1R_1}+\frac{1}{C_2R_2}+\frac{1-A_{HP}}{C_1R_1}\right)+\frac{1}{C_1C_2R_1R_2}}$$

Where $A_{HP}=1+R_3/R_4$

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Condition	Min	Max
Power Supply Voltage (V_{DD} to Vss)	-0.5V	+7V
Analog Input Voltage (IN+ or IN-)	Vss-0.5V	V_{DD}+0.5V
PDB Input Voltage	Vss-0.5V	+7V
Operating Temperature Range	-40°C	+125°C
Junction Temperature	+150°C	
Storage Temperature Range	-65°C	+150°C
Lead Temperature (soldering, 10sec)	+300°C	
Package Thermal Resistance (T_A=+25°C)		
SOP23-5, θ_{JA}	190°C	
SOP8, θ_{JA}	130°C	

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Electrical Characteristics

(V_{DD} = +5V, Vss = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L=100K tied to V_{DD}/2, SHDNB = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A =+25°C.) (Notes 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply-Voltage Range	V_{DD}	Guaranteed by the PSRR test	2.2	-	5.5	V
Quiescent Supply Current (per Amplifier)		V_{DD} = 5V	-	320	380	μA
Input Offset Voltage	V_{OS}		-	-	±15	μV
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$		-	-	0.05	μV/°C
Input Bias Current	I_B	(Note 2)	-	80	-	pA
Input Offset Current	I_{OS}	(Note 2)	-	80	-	pA
Input Common-Mode Voltage Range	V_{CM}		-0.1	-	V_{DD}+0.1	V
Common-Mode Rejection Ratio	CMRR	V_{DD}=5.5 Vss-0.1V≤V_{CM}≤V_{DD}+0.1V	90	110	-	dB
		Vss≤V_{CM}≤5V	100	120	-	dB
Power-Supply Rejection Ratio	PSRR	V_{DD} = +2.5V to +5.5V	90	110	-	dB
Open-Loop Voltage Gain	A_V	V_{DD}=5V, R_L=100kΩ, 0.05V≤V_O≤4.95V	110	130	-	dB
Output Voltage Swing	V_{OUT}	$\lvert V_{IN+}-V_{IN-}\rvert \geq$ 10mV $V_{DD}-V_{OH}$	-	6	-	mV
		R_L = 100kΩ to V_{DD}/2 $V_{OL}-V_{SS}$	-	6	-	mV
		$\lvert V_{IN+}-V_{IN-}\rvert \geq$ 10mV $V_{DD}-V_{OH}$	-	60	-	mV
		R_L = 5kΩ to V_{DD}/2 $V_{OL}-V_{SS}$	-	60	-	mV
Output Short-Circuit Current	I_{SC}	Sinking or Sourcing	-	±15	-	mA
Gain Bandwidth Product	GBW	A_V = +1V/V	-	1.5	-	MHz
Slew Rate	SR	A_V = +1V/V	-	0.4	-	V/μs
Settling Time	t_S	To 0.1%, V_{OUT} = 2V step A_V = +1V/V	-	20	-	μs
Over Load Recovery Time		V_{IN} × Gain=V_S	-	100	-	μs
Input Voltage Noise Density	e_n	f = 1kHz	-	15	-	nV/√Hz
		f = 100Hz	-	16	-	

Note 1: All devices are 100% production tested at T_A = +25°C; all specifications over the automotive temperature range is guaranteed by design, not production tested.

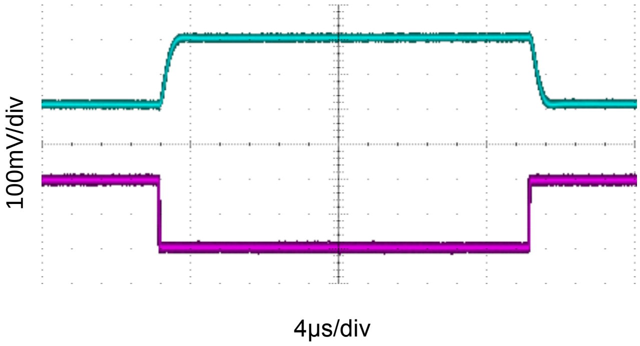
Note 2: Parameter is guaranteed by design.

6.3 Typical characteristics

At T_A=+25°C, R_L=10 kΩ connected to V_S/2 and V_{OUT}= V_S/2, unless otherwise noted.

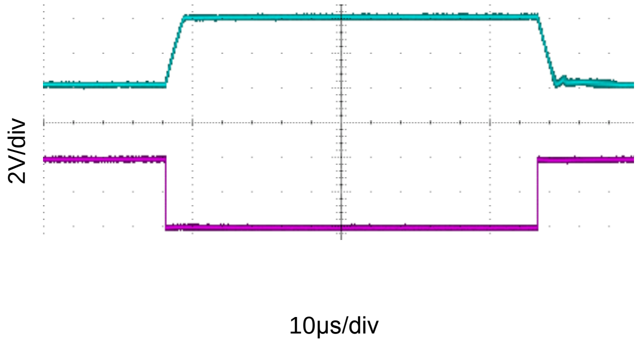
Small Signal Step Response

G=-1V/V,R_L=10kΩ,C_L=100pF



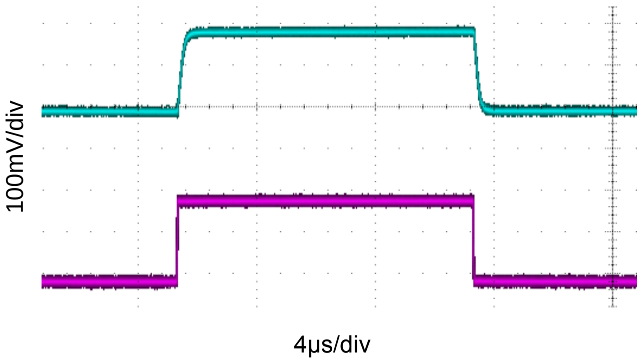
Large Signal Step Response

G=-1V/V,R_L=10kΩ,C_L=100pF



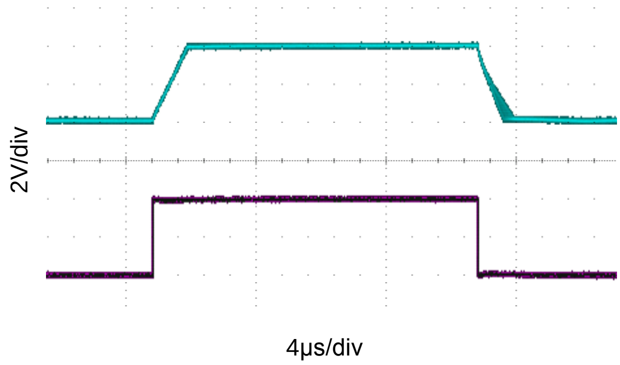
Small Signal Step Response

G=+1V/V,R_L=10kΩ,C_L=100pF



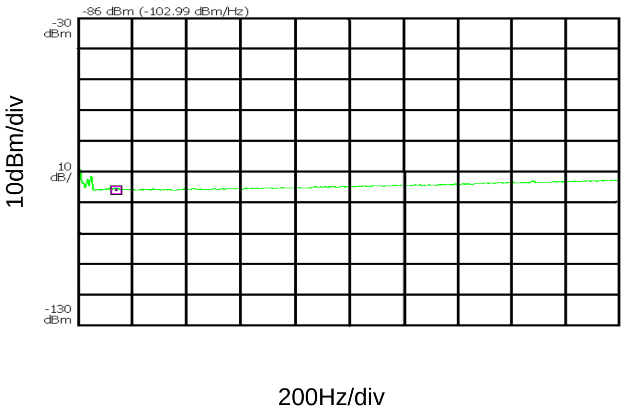
Large Signal Step Response

G=+1V/V,R_L=10kΩ,C_L=100pF



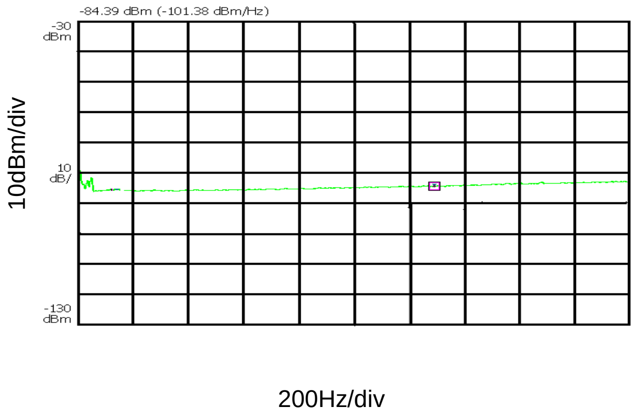
Input Voltage noise Spectral Density VS. Frequency

Noise Gain=101,V_n=15.6(nV/√Hz)@200Hz



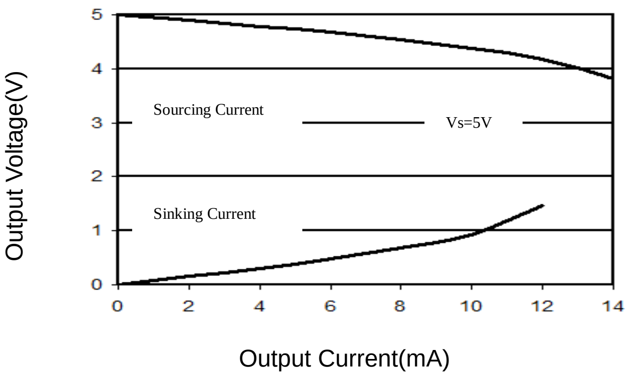
Input Voltage noise Spectral Density VS. Frequency

Noise Gain=101,V_n=18.8(nV/√Hz)@1KHz

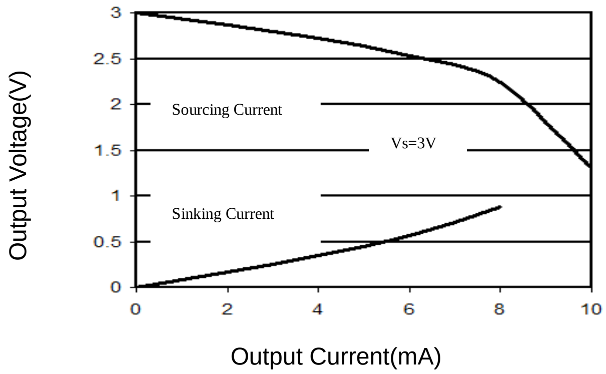


At T_A=+25°C, R_L=10 kΩ connected to V_S/2 and V_{OUT}= V_S/2, unless otherwise noted.

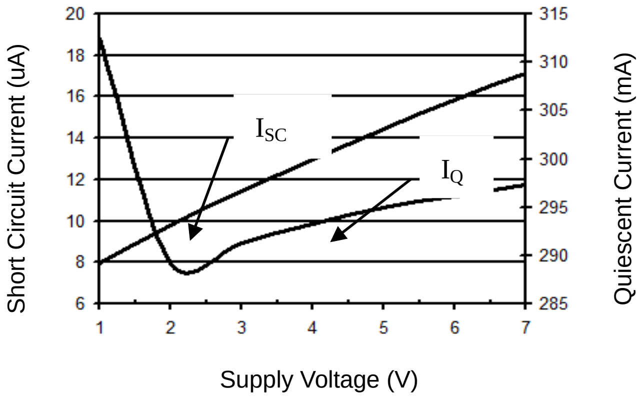
Output Voltage Swing vs. Output Current



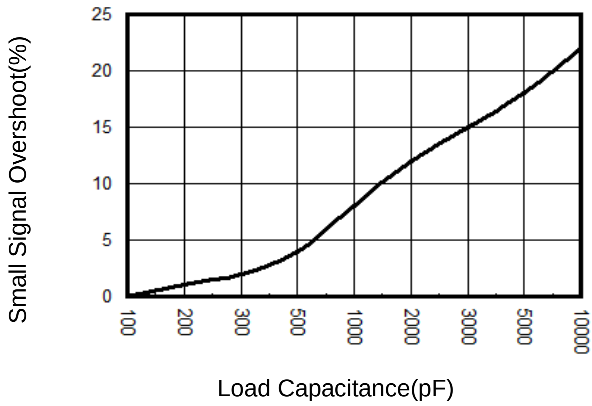
Output Voltage Swing vs. Output Current



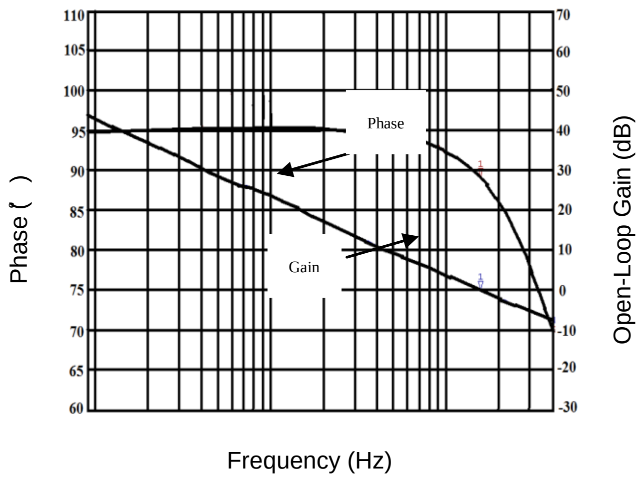
Quiescent and Short-Circuit Current Vs. Supply Voltage



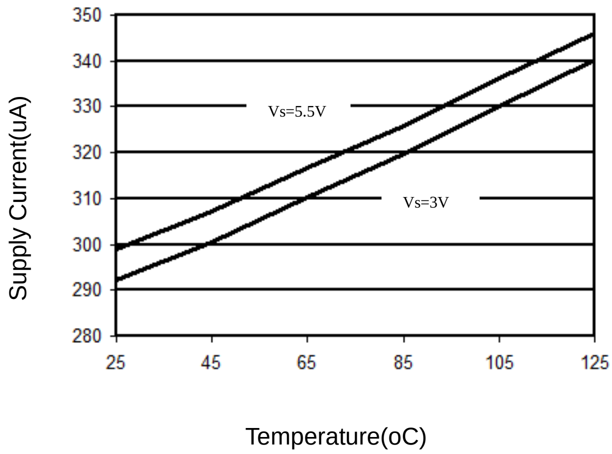
Small Signal Overshoot vs. Load Capacitance



Open-Loop Gain And Phase VS. Frequency



Supply Current vs. Temperature



7. Ordering Information

GT XXXX - XX X X

Temperature Range

I Industrial: -40°C~+125°C

Pb Status

G GREEN

Package Type:

TF SOT23-5
G SOP8

Part Number

Giantec Prefix

GT Giantec

Order Number	Package Description	Package Option
GT7161-TFGI-TR	SOT23-5	Tape and Reel 3000
GT7161-GGI-TR	SOP8	Tape and Reel 4000

8. Part Markings

8.1 GT7161-TFGI (Top View)

1	6	1	Y	W

161	GT7161-TFGI		
●	Pin 1 Indicator		
Y	Seal Year	**W**	Seal Week
2010 (1st half year)	A	Week 01	A
2010 (2nd half year)	B	Week 02	B
2011 (1st half year)	C	……	
2011 (2nd half year)	D	Week 26	Z
2012 (1st half year)	E	Week 27	A
2012 (2nd half year)	F	Week 28	B
……	……	……	……
2022 (2nd half year)	Z	Week 52	Z

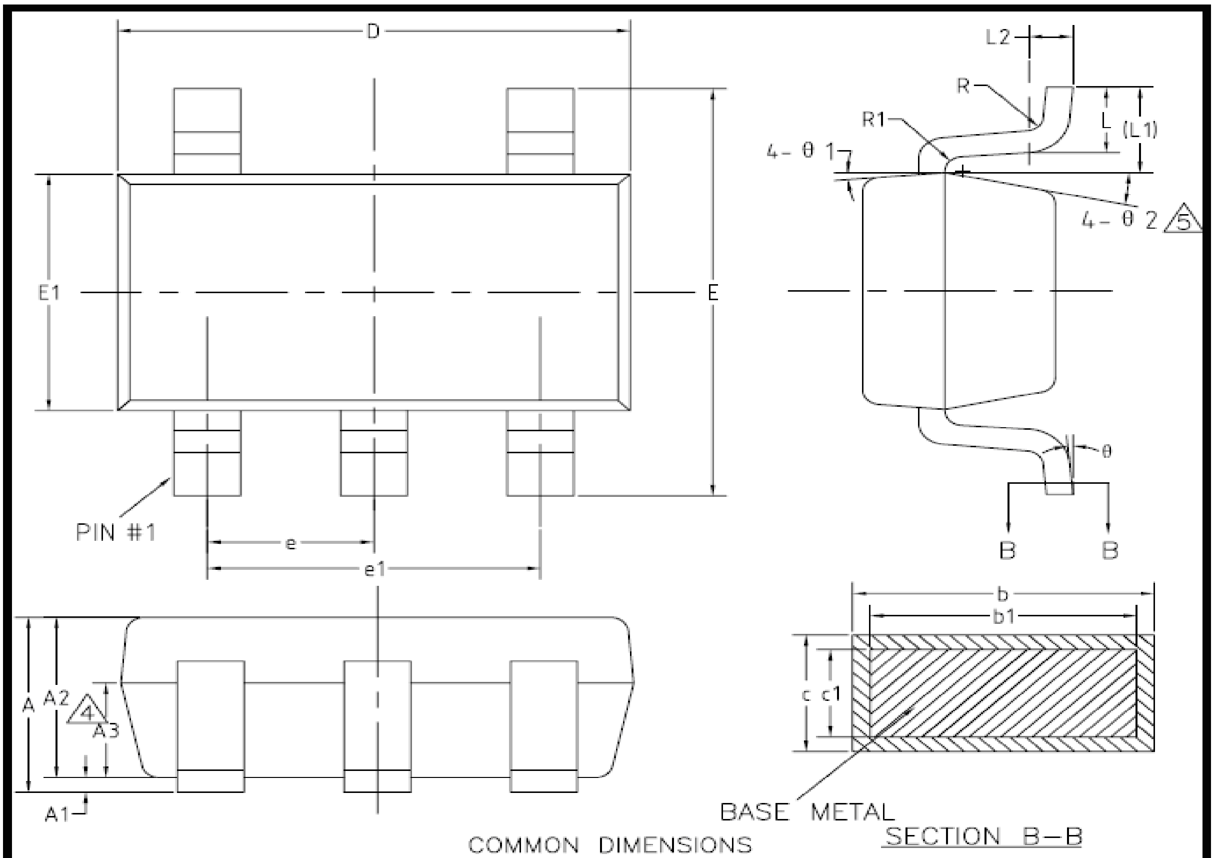
8.2 GT7161-GGI (Top View)

G	T	7	1	6	1	G	G	I
				Lot Number				
●		Y	Y	W	W	S	V	

GT7161GGI	
Lot Number	States the last 9 characters of the wafer lot information
●	Pin 1 Indicator
YY	Seal Year
	00 = 2000
	01 = 2001
	99 = 2099
WW	Seal Week
	01 = Week 1
	02 = Week 2
	.
	.
	.
	51 = Week 51
	52 = Week 52
S	Subcon Code
	J = ASESH
	L = ASEKS
V	Die Version

9. Package Information

9.1 SOP23-5

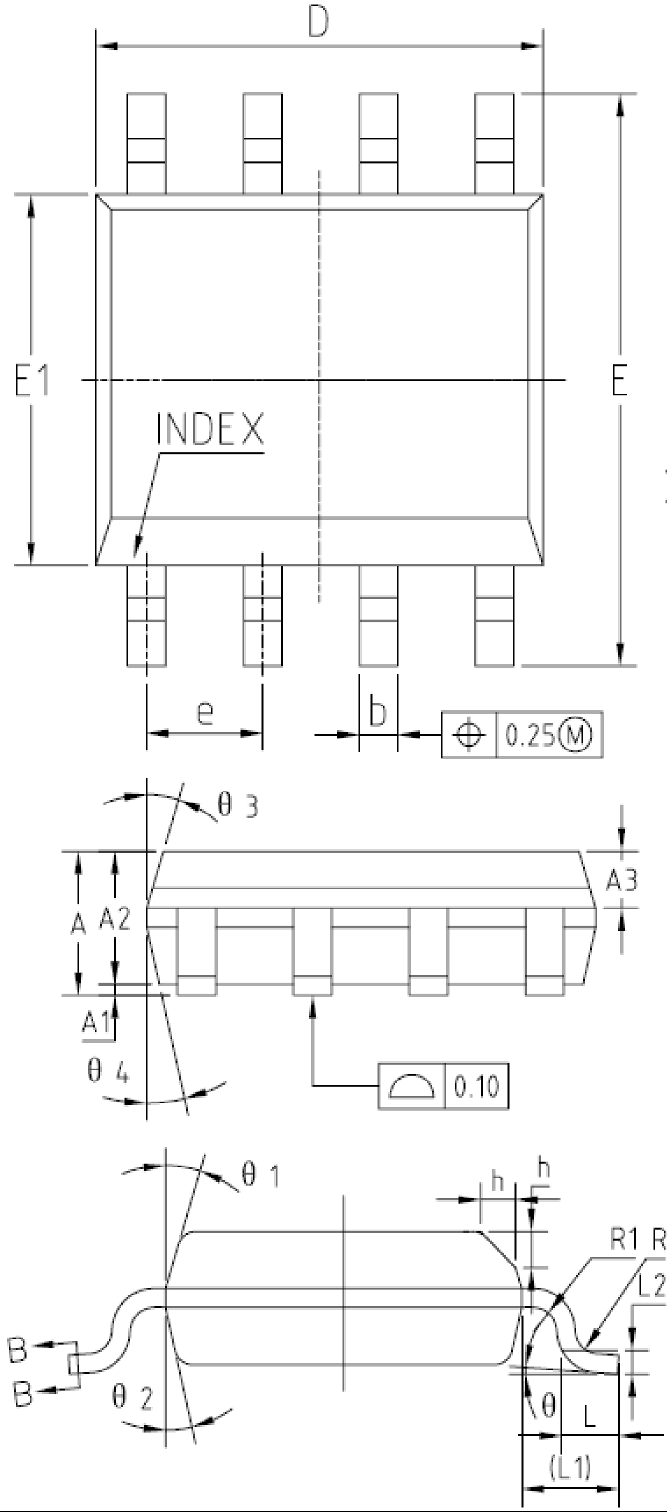


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

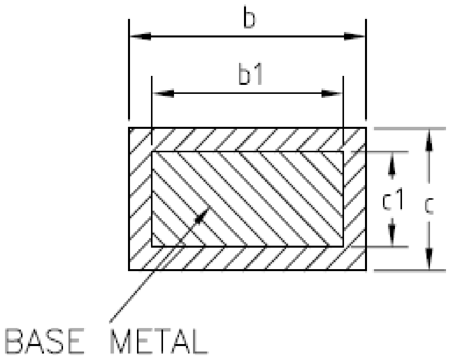
	SYMBOL	MIN	NOM	MAX
	A	—	—	1.25
3	A1	0	—	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
	b	0.36	—	0.50
	b1	0.36	0.38	0.45
	c	0.14	—	0.20
	c1	0.14	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
	E1	1.526	1.626	1.726
5	e	0.90	0.95	1.00
5	e1	1.80	1.90	2.00
	L	0.35	0.45	0.60
	L1	0.59REF		
	L2	0.25BSC		
	R	0.10	—	—
	R1	0.10	—	0.25
	θ	0°	—	8°
	θ 1	3°	5°	7°
5	θ 2	6°	—	14°

9.2 SOP8



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	–	0.51
b1	0.37	0.42	0.47
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ 1	15°	17°	19°
θ 2	11°	13°	15°
θ 3	15°	17°	19°
θ 4	11°	13°	15°



10. Revision History

Revision	Date	Descriptions
A0	Sept.,2011	Initial Version