1. Introduction

This application note provides assistance and guidance on how to use GIANTEC I^2C serial EEPROM products. The following topics are discussed one by one:

- Power supply & power on reset
- Power saving
- IO Configuration
- Check completion of Write Cycle
- Write-protect application
- GT34TS02 temperature sensors application
- Data throughput
- Schematic of typical application
- Recommendation of PCB Layout
- Reference design of software

2. Power supply & power on reset

GIANTEC 34 series EE products work well under stable voltage within operating range specified in datasheet respectively. For a robust and reliable system design, please pay more attention to the following items:

2.1 Ensure VCC stable

In order to filter out small ripples on VCC, connect a decoupling capacitor (typically 0.1μf) between VCC and GND is recommended (Shown in figure 1). In addition, it is recommended to tie the pull-up resistor to the same VCC power source as EEPROM, if MCU is powered by a different VCC power source.

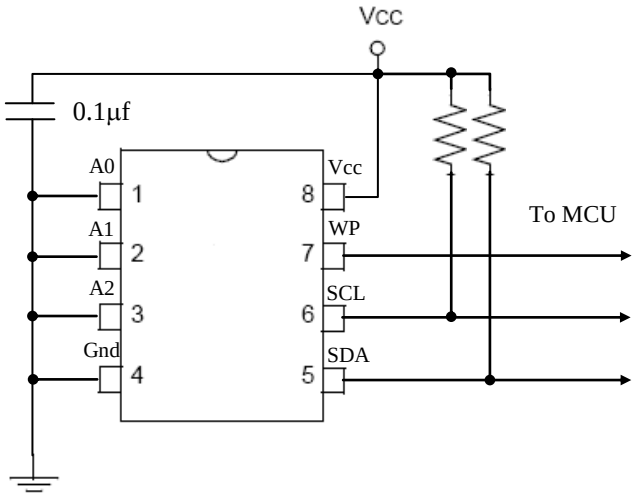

Figure 1: GIANTEC GT34C02 EEPROM recommended connections

2.2 Power on reset

During power ramp up, once VCC level reaches the power on reset threshold, the EEPROM internal logic is reset to a known state. While VCC reaches the stable level above the minimum operation voltage, the EEPROM can be operated properly. Therefore, in a good power on reset, VCC should always begin at 0V and rise straight to its normal operating level, instead of being at an uncertain level. Shown in figure 2. Only after a good power on reset, can EEPROM work normally. The operating range of VCC can be found in the datasheet. It is recommended to do software reset by MCU immediately after POR to further ensure the proper initialization of the device.

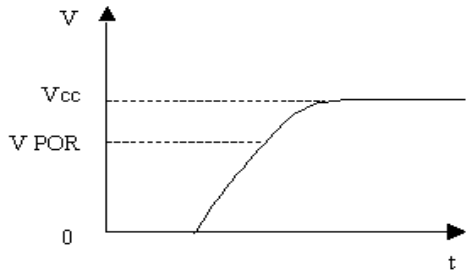

Figure 2: Power on reset

2.3 Power down

During power down, the minimum voltage level that VCC must drop to prior resume back to the normal operating level is 0.2V to ensure the proper POR process, Shown in figure 3

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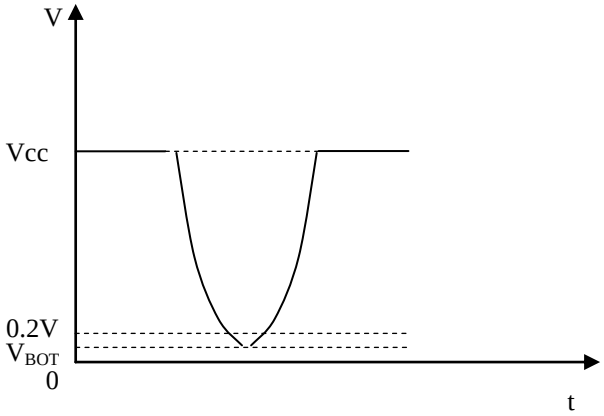


Figure 3: Power Down

2.4 Software reset

In case of no way to know the current state of EEPROM or want to cancel the current operation of EEPROM, usually software reset is used to make EEPROM enter standby mode, but software reset cannot reset the internal address counter of EEPROM device. Software reset is caused by a START condition that is sent by master device. During the process of EEPROM read/write operation, whenever recognizes the START condition, current operation will be stopped. However, the following cases need to be considered:

1) Master device sends a START condition while the EEPROM is executing a read instruction and sending bit "0" to master device, because SDA is being driven low by EEPROM, EEPROM cannot recognize this START condition and thus cannot make software reset happen. In order to solve this kind of issue, master device need to send nine sequential bits "1" after START condition, thus EEPROM will not be able to get the response from master device, therefore force an internal reset to be generated, Shown in figure 4.

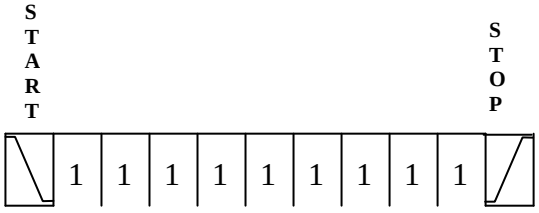


Figure 4: Software reset

2) Master device sends a START condition while the EEPROM is acknowledging a WRITE instruction and is driving SDA low, even though the master device sends nine sequential bits "1", the EEPROM cannot be reset. In this case, master device need to send a START condition after nine sequential bits "1" to make EEPROM reset, Shown in figure 5.

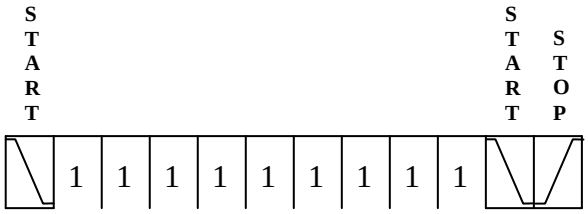


Figure5: Software reset

After device internal reset, master device may send a STOP condition to bring EEPROM into standby mode. Therefore, a full reliable software reset process will comprise a START condition, 9 sequential bits "1", a START condition and a STOP condition. The reference code can be found in chapter 10.

3. Power saving

To reduce the power consumption, the following cases need to be considered:

3.1 Whenever no need to operate EEPROM, bring it into standby mode. In this mode, the power consumption is minimum correspondingly. Following cases can bring EEPROM into standby mode:
   1) After power-up, and remain this state until SCL or SDA toggles;
   2) Recognize a STOP signal after a non-read operation is initiated;
   3) Completion of internal write operation.

3.2 Usually, pull-up or pull-down resistor contributes to power consumption too. Under the same conditions, big resistor consumes less power, and small resistor consumes more power;

3.3 The power consumption is maximum correspondingly during its write cycle. If a large amount of data needs to be written into the EEPROM, definitely the page write mode consumes less time and power than byte write mode. Therefore, if there are a lot of data to be written, the page write mode should be used instead of byte write mode. If there are a lot of data to be read, the sequential read mode will be recommended. The sequential read mode can improve the read efficiency and reduce the power consumption as well.

4. IO Configuration

In order to reduce the possibility of wrong operation inadvertently due to noise, it is recommended that SDA pin and SCL pin should be tied to a proper pull-up resistor to improve the anti-jamming capability of EEPROM. If the pull-up resistors are not used in a ready-made application, it is recommended to set SCL and SDA high after POR. It will bring EEPROM into a known high-level state after POR. In general applications, the pull-up resistor needs to be considered at the beginning of design according to following suggestion:

1) Since pull-up resistor affects the coupling capacitor on SDA bus as well as the rise time of SDA, thus it will impact the bus transmission efficiency. For example, if read operation is executed quickly enough, SDA will be sampled already by MCU before it rises to stable high level, then MCU may get the wrong data. To solve these kinds of issues, the frequency of SCL need to be reduced. Usually reducing the MCU frequency or adding a fixed delay during the read operation will help a lot, however, meantime the transmission efficiency between MCU and EEPROM will be reduced too. Therefore, another way may be used to speed up bus rising time, technical speaking, small pull-up resistor will make SDA bus rise more quickly than big pull-up resistor, thus data transmission efficiency will be higher as well. In

general application, it is recommended to select pull-up resistor from 1.5k to 3.5k for fast mode and 3.5K to 12K for standard mode.

2) Technical speaking, only if the MCU IO pin which is tied to SCL is in open drain mode, a pull-up resistor is need by SCL, but in order to reduce the noise on SCL after POR, always it is recommended to tie a proper pull-up resistor to SCL. This will be helpful to make EEPROM device enter a known stable high-level state after POR. The pull-up resistor's value is recommended to be same with the pull-up resistor value on SDA.

5. Check completion of Write Cycle

Definitely, effective checking of the completion of write cycle will improve the efficiency of the write operation. Once recognize a STOP condition, EEPROM will start its internal write cycle, and then the checking for write cycle can be started. The steps for checking completion of write cycle are listed as below:

1) Send a dummy write operation to EEPROM, the dummy write operation includes a START condition and a slave address, shown in figure 6.

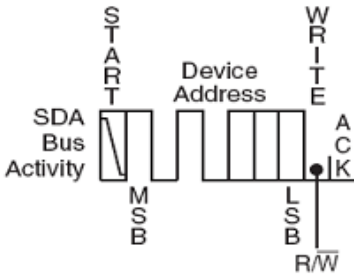


Figure 6: Dummy write operation

2) Poll ACK returned from EEPROM. If the write cycle is over, the ACK will be returned, if the write cycle is underway, the ACK will not be returned and step 1 and step 2 need to be repeated until the write cycle is over.

The referenced code can be found in chapter 10.

6. Write-protect application

GIANTEC 34 series EEPROM include GT34C02 EEPROM and GT34TS02 EEPROM. They provide software write protection function, but only GT34C02 EEPROM provides hardware write protection function. Details are as follows:

1. Hardware write protection

GIANTEC GT34C02 EEPROM provides hardware write protection function. This function can be enabled or disabled depends WP pin, if WP is high, the hardware write protection function is enabled and the write operation on EEPROM will be ignored, if WP is low or floating, the hardware protection function is disabled and the write operation on EEPROM is valid. In general applications, WP can be tied to VCC, GND or IO pin of MCU. If the write protection function is controlled by software, it is recommended to drive WP high or low and keep WP stable before the START condition of write operation. This will help EEPROM to check whether the write protection function is enabled or not in time.

2. Software write protection

GIANTEC GT34C02 and GT34TS02 EEPROM provide software write protection function. You can send specific instructions to enable the software write protection. The first 128 bytes memory can be write-protected either permanently or reversible. Detailed instructions are as shown in table 1.1.

Memory Area Function	Slave Address							
	D3	D2	D1	D0	A2	A1	A0	R/W
SWP	0	1	1	0	0	0	1	0
CWP	0	1	1	0	0	1	1	0
PSWP	0	1	1	0	A2	A1	A0	0
Read SWP	0	1	1	0	0	0	1	1
Read CWP	0	1	1	0	0	1	1	1
Read PSWP	0	1	1	0	A2	A1	A0	1

Table 1.1

Please note as follows:

1) For GT34C02, if you want to send SWP, CWP, PSWP instruction to EEPROM, please set the WP to 0.
2) The first 4 bit of the slave address is 0110.Others the software write protection have specific requested to A0, A1, A2. Detailed requirement see table 1.1.
3) The software write protection have two data protection feature to lock the data in its first half 128 bytes (address ooh to 7fh). One of the features is to permanently lock. The other is to reversible lock.

7. GIANTEC GT34TS02 temperature sensors application

GIANTEC GT34TS02 is a new Temperature Sensors product. For its application , please note as follows:

1) Any illegal operations or write to invalid/reserved registers is prohibited.
2) The first 4 bit of the slave address is 0011.
3) The registers selected by pointer register.
4) After power on, configuration steps on the register as follows:
    a) Configured Upper/Lower Alarm Window register and Critical Limit register.
    b) Configured Capability register.
    c) Configured Configuration register.

8. Data throughput

To improve the data throughput, the following solutions are recommended:

1) In order to improve the data throughput, hardware-wise, the operation frequency between MCU and EEPROM may be improved, for example, a faster MCU or a higher frequency oscillator may be chosen, software-wise, the delay between SCK transitions need be reduced, those instructions which need less machine cycles will be preferred, for example, SETB can save a machine cycle time comparing with MOV. The pull-up resistor value on SDA need also be chosen as smaller as possible to match the MCU operation speed, but this way will increase the power consumption.
2) The page write mode is recommended to write a large amount of data instead of byte write mode. The page write mode consumes less time than byte write mode, so it can improve the transmission efficiency;
3) The sequential read is recommended to read serial data instead of byte read. The sequential read consumes less time than byte read, so it can improve the transmission efficiency;
4) While an internal write cycle is underway, please consider the solution recommended in chapter 5 to check if write cycle is over. The traditional fixed delay solution always consumes more time and thus reduces the transmission efficiency.

9. Schematic of typical application

1) If there is only one EEPROM on I^2C bus, the recommended connection is shown in figure 1. If WP needs not to be controlled by MCU, the WP pin can be tied to GND (hardware protection disabled) or VCC (hardware protection enabled).
2) If there are several EEPROM devices on I^2C bus, the connection is similar to previous case. The difference is that each EEPROM need to be set an address, A0, A1 and A2 need to be configured.

Shown in figure 7, the address is from 0 to 7 respectively as the order from left to right. If master device need access one device of them, A0, A1 and A2 bit in slave address need to be configured properly, then the corresponding EEPROM device can be accessed. The format of slave address is shown in figure 8. For example, if A0, A1 and A2 of some EEPROM are set as *high, high and low* respectively, the slave address should be binary format "10100110".

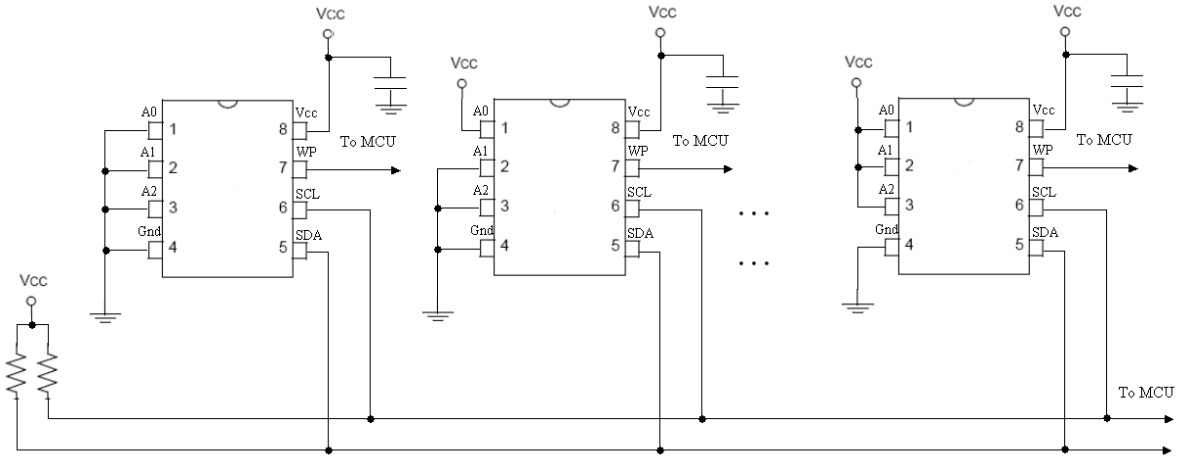


Figure 7: Several EEPROM on a bus

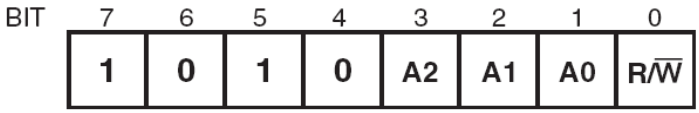
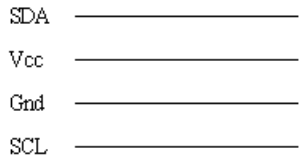


Figure 8: Slave address

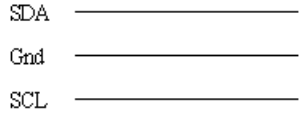
10. Recommendation of PCB Layout

In order to reduce the crosstalk interference on I^2C bus, it is recommended to lay SDA line and SCL line in pairs. The wire length of SDA and SCL is recommended to lay as shorter as possible. The longer wire and crossed wire should be avoided. If PCB size is large enough, the GND line should be lay in the middle of these bus lines. If the length of the bus lines exceeds 10 cm, the recommended wiring pattern is listed as below:

1) Bus with VCC and GND together:

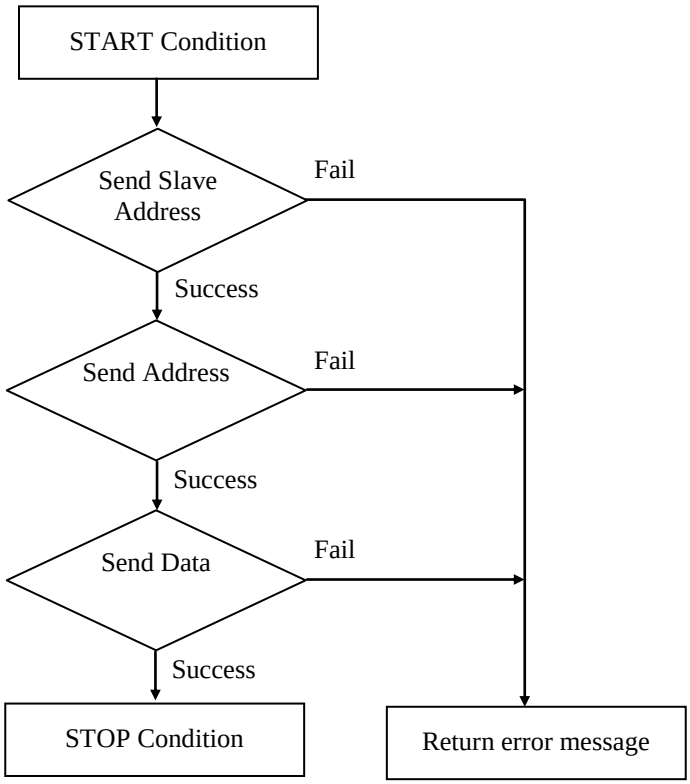


2) Bus with only the GND together:

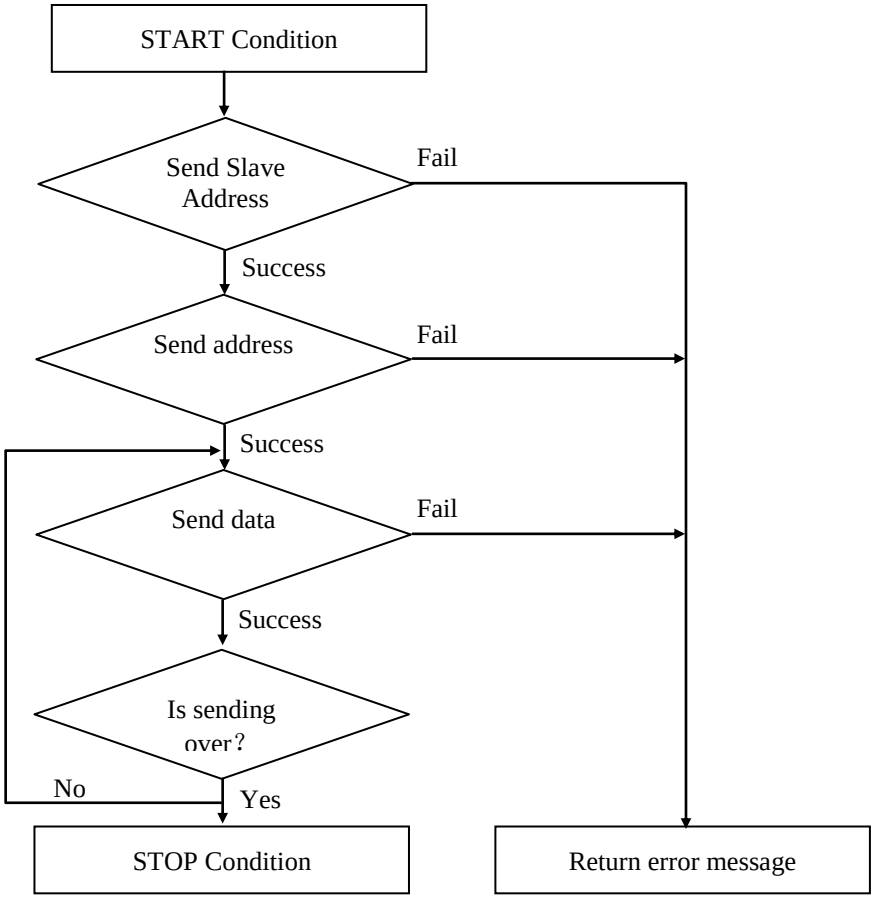


11. Reference design of software

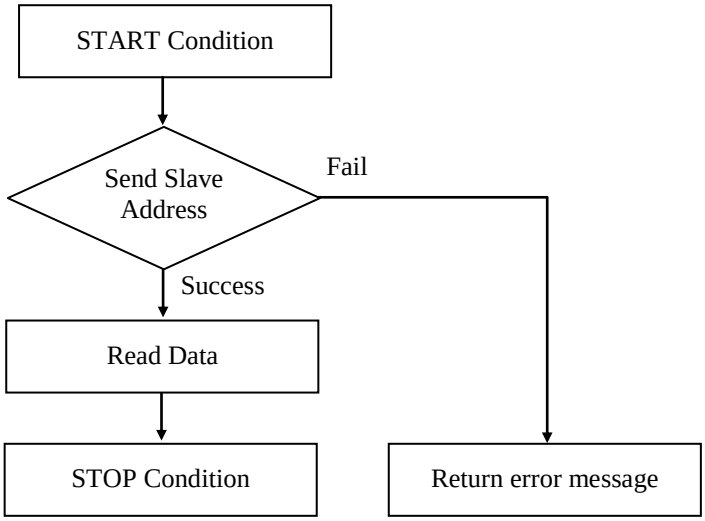
10.1 Byte write flow chart



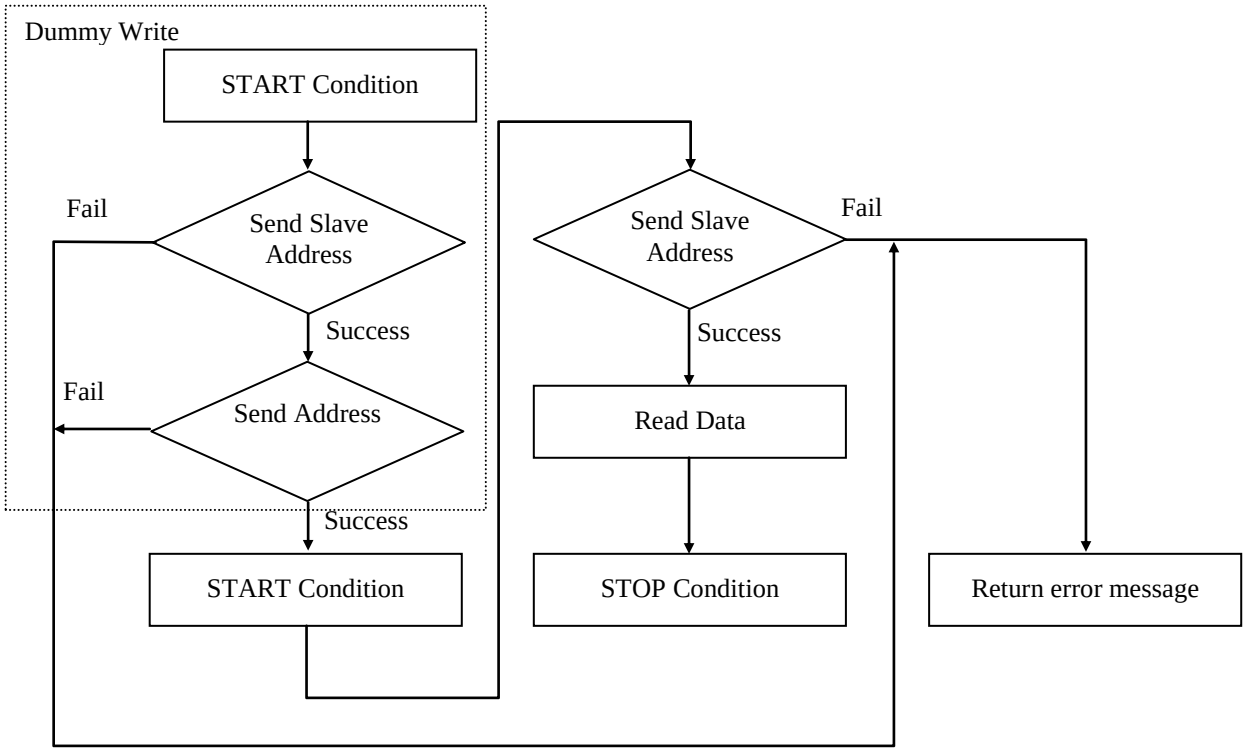
10.2 Page write flow chart



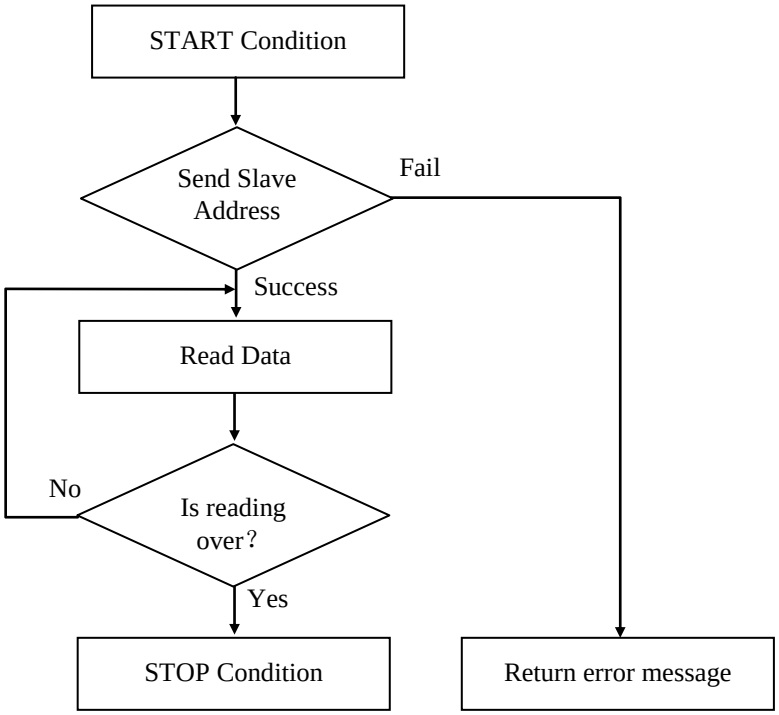
10.3 Current address read flow chart



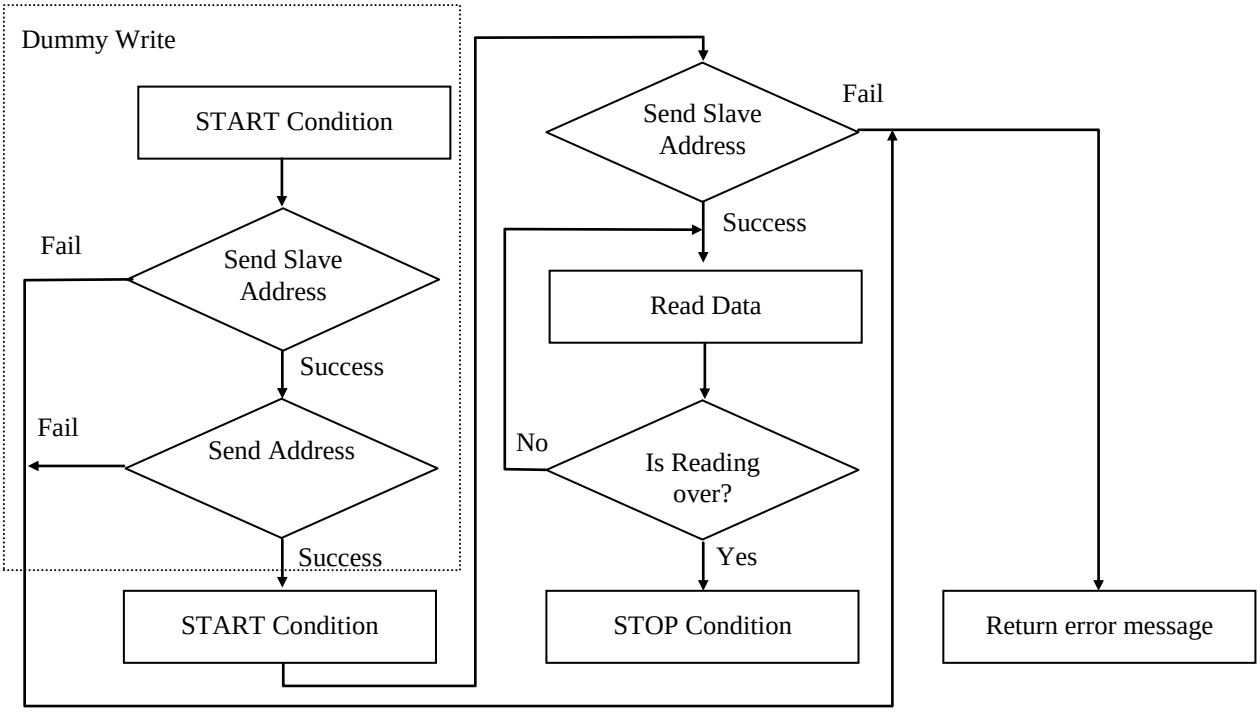
10.4 Random address read flow chart



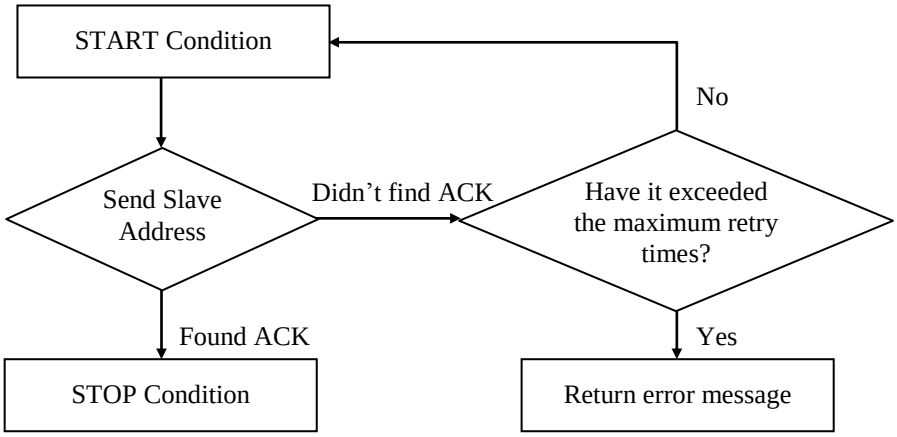
10.5 Current address sequential read flow chart



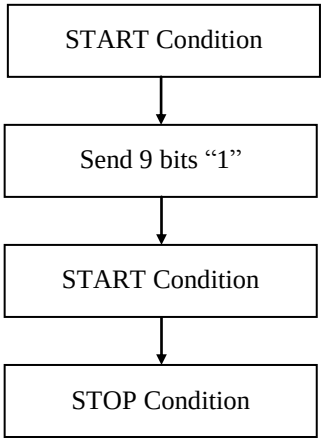
10.6 Random address sequential read flow chart



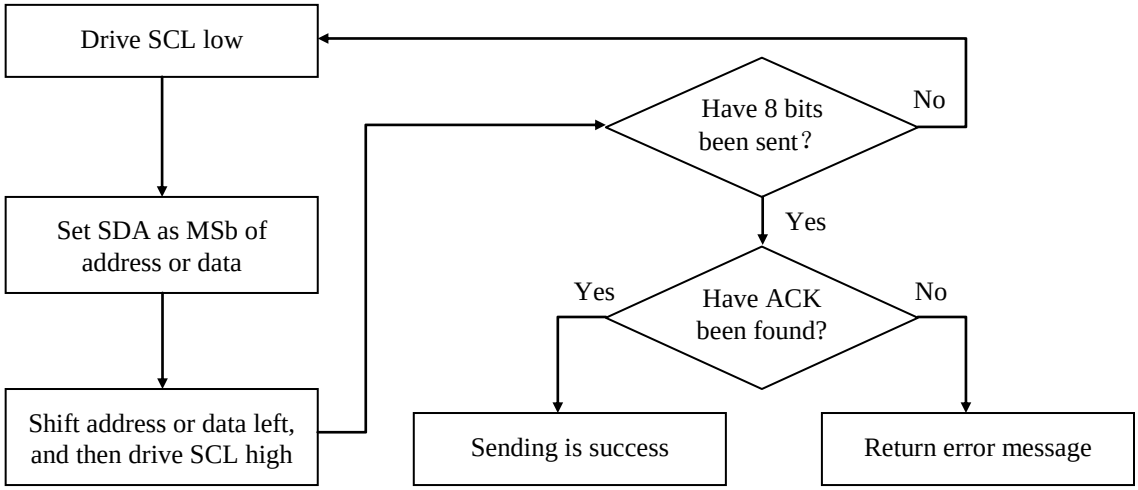
10.7 Write Cycle polling flow chart



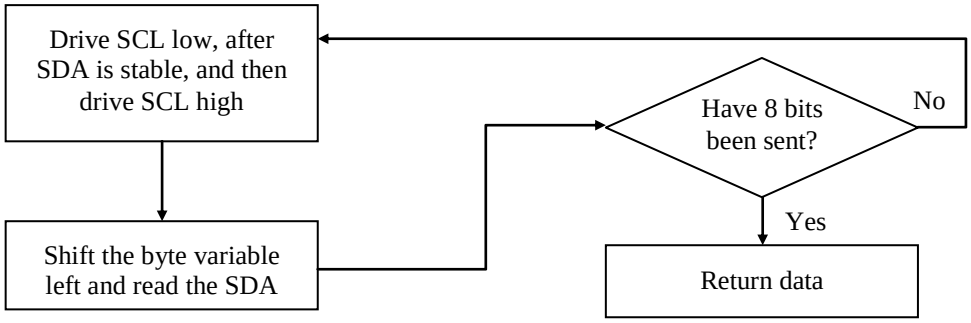
10.8 Software reset flow chart



10.9 Shift bit out flow chart



10.10 Shift bit in flow chart


Drive SCL low, after SDA is stable, and then drive SCL high
Shift the byte variable left and read the SDA
Have 8 bits been sent?
No
Yes
Return data